Group Report

1964-25

Haystack-West Ford Intersite Coupling Link

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14 May 1964

Prepared under Electronic Systems Division Contract AF 19(628)-500 by

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts

The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology, with the support of the U.S. Air Force under Contract AF 19(628)-500.

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LINCOLN LABORATORY

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ABSTRACT

This report describes the Haystack-West Ford Intersite Coupling Link which permits the West Ford antenna to be pointed with data obtained from the Univac 490 computer at Haystack. A detailed description of the logic is presented preceded by a general description of the system.

Accepted for the Air Force
Franklin C. Hudson, Deputy Chief
Air Force Lincoln Laboratory Office

HAYSTACK-WEST FORD INTERSITE COUPLING LINK

I. GENERAL

The Haystack-West Ford Intersite Coupling Link permits the West Ford antenna to be pointed with commands generated by the Univac 490 computer located at Haystack. The Link consists of a computer interface and a data transmitter at Haystack and a data receiver at West Ford; the transmitter and receiver are connected by two telephone lines.

The Link transmits Azimuth, Elevation, Doppler, and Range commands to the West Ford antenna pointing equipment* in serial form over one of the telephone lines at a 2-Kc bit rate. The data are obtained from channel 12 on the 490 in sets of three 30-bit words with the format shown in Fig. 1. The two most significant bits are used as identity tags which permit the data transmitter and receiver to recognize each word; the "ones" in bits 15, 16, and 17 of the Range word are used to prevent full transmission of this word, as only the lower order bits contain meaningful information.

Timing for the Link is based on the 20-cps cycle time of the West Ford pointing equipment which is asynchronous with the Haystack clock. Consequently, the Link must establish synchronization whenever data transmission is initiated.

Figure 2 shows the timing for the transmission of a typical set of data (assuming synchronization has been established). A 20-cps signal is sent from West Ford to Haystack (via the second telephone line) to initiate transmission of each data set. This signal generates an Output Data Request (ODR) signal in the data transmitter which informs the computer that data is desired. The computer has in storage a table of 120 words (2 seconds worth of data) arranged in order (AZ/EL, DOPPLER, RANGE, AZ/EL, DOPPLER, RANGE, ... etc.) and at some variable time (on the order of a few 10's of microseconds) after receipt of the ODR, an AZ/EL word is sent out on channel 12 accompanied by an Acknowledge (ACK) signal. The word is then loaded into the data transmitter which generates a sync bit and then transmits the data over the telephone line. Upon completion of data transmission, the data transmitter sends a parity bit over the line and generates a second ODR. The computer acknowledges this ODR by transferring a Doppler word to the data transmitter. The transmitter again generates

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*F. E. Heart and A. A. Mathiasen, Proc. IEEE (May 1964). (In Preparation) For more detail, see "Digital Antenna Aiming System," Lincoln Manual No. 50 (July 1962).

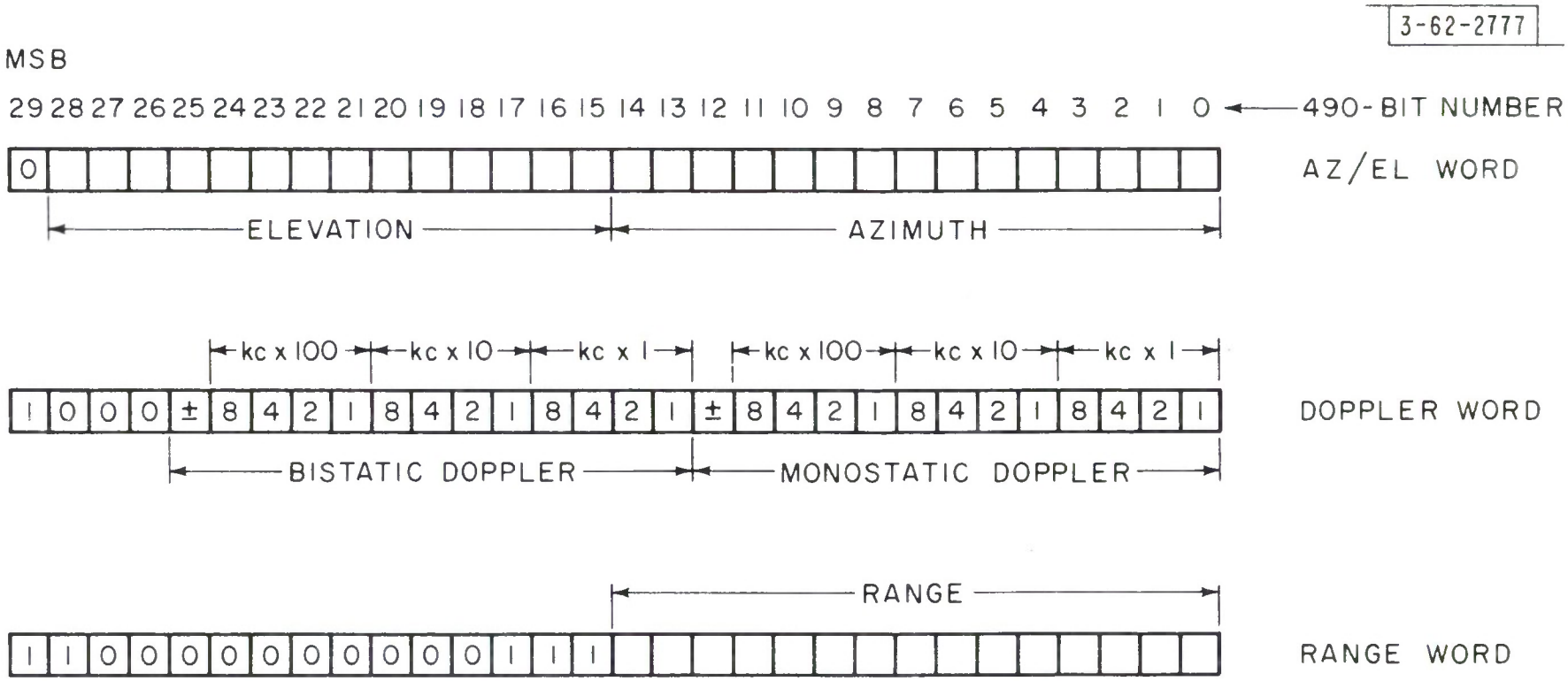


Fig. 1. 490 Word Format

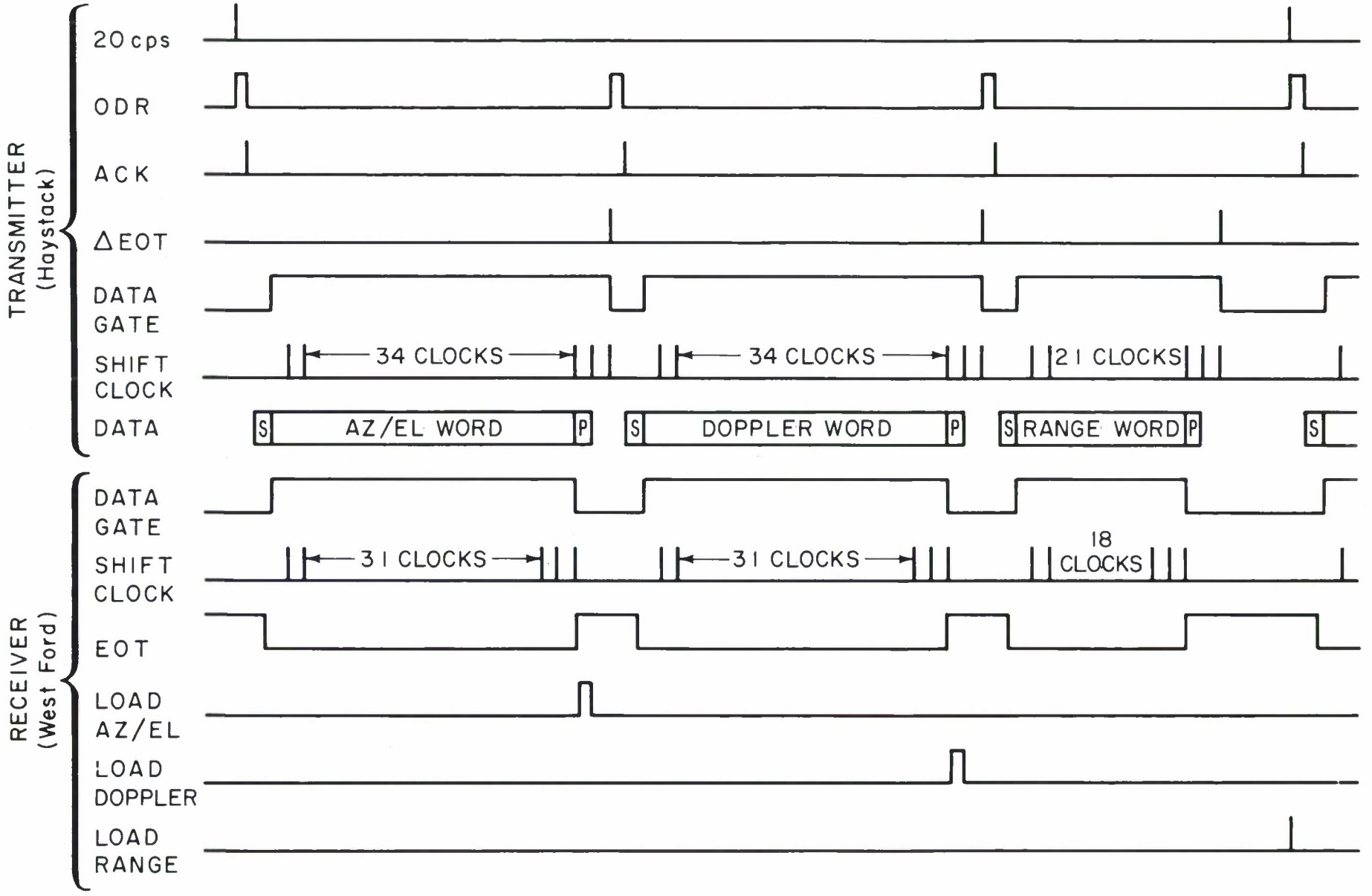


Fig. 2. Data Transmission Cycle Timing

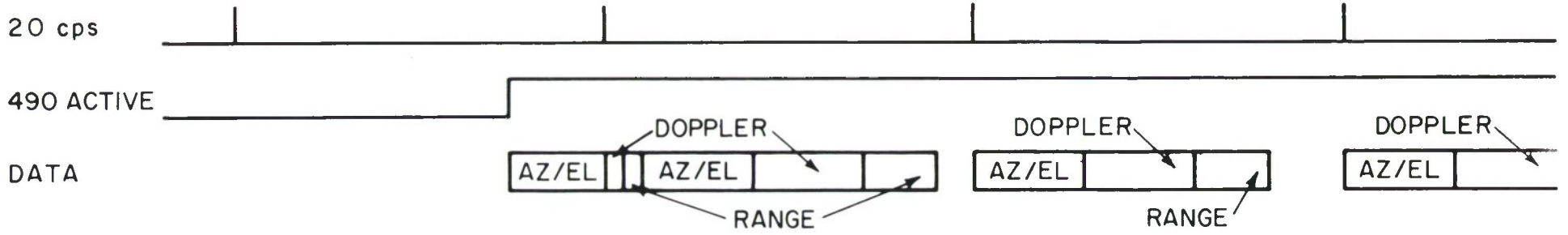
a sync bit and then transmits the data followed by a parity bit. After transmitting this word, the transmitter generates a third ODR, and the computer transfers a Range word to the data transmitter. This word is sent over the telephone line in similar fashion, and the data transmitter then waits for the next 20-cps signal to initiate another transmission cycle.

The arrival of the first word (AZ/EL) at the data receiver is signalled by the occurrence of the first sync bit which clears the data receiver. The data is then shifted in until the word is fully loaded, at which time the data is transferred to the Azimuth and Elevation command registers in the West Ford pointing equipment, provided that the identity tag and parity are correct (and also that the mode switch at the West Ford site is in the intersite coupling position).

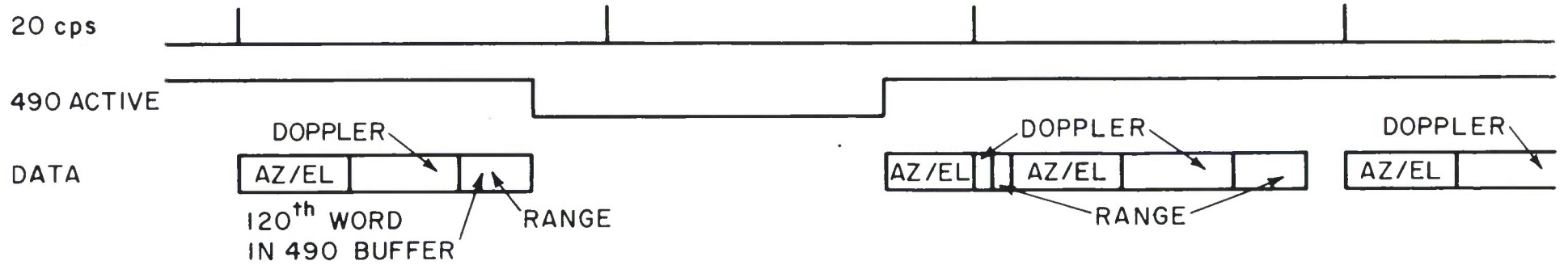
The arrival of the next sync bit again clears the receiver to permit the Doppler word to be shifted in. Again, provided that the identity tag and parity are correct, this word is loaded into the Doppler display register in the West Ford equipment.

The range word is processed in the same manner with the exception that transfer to the Range command register does not take place until the occurrence of the next 20-cps signal.

Figure 3. a illustrates the synchronization process that occurs whenever data transmission is initiated. Prior to initiation, 20-cps signals will have occurred steadily, and, therefore, the ODR signal will be set awaiting an acknowledge signal from the computer. This acknowledge will occur within microseconds after the computer activates channel 12, and, because of the asynchronous nature of the system, this can occur at any time relative to the 20-cps signals. (The computer is activated on an even second as measured by the Haystack clock.) The illustration shows one possible timing relationship; in this case, the next 20-cps signal after the first acknowledge occurs while the AZ/EL word is being transmitted. The ODR is set by this 20-cps signal and the computer transfers out the next word; in this case, a Doppler word. The data transmitter expects to get an AZ/EL word whenever it generates an ODR with a 20-cps signal, and, therefore, when it reads the identity tag on a Doppler word, it rejects it and immediately resets the ODR. The computer then acknowledges this ODR and sends out the next word (range). Again, the data transmitter rejects it and resets the ODR. The next word is then transferred from the computer, and, since it is an AZ/EL word, a normal data transmission cycle takes place. Normal cycles now continue (the system is synchronized) until the computer buffer is emptied. In the particular case being considered, the buffer is emptied in



(a) INITIAL SYNCHRONIZATION



(b) RESYNCHRONIZATION

Fig. 3. (a) Initial Synchronization

(b) Resynchronization

less than two seconds since the data transmitter discarded two words. The buffer is reloaded by the computer every two seconds as measured by the Haystack clock, and, therefore, essentially the same timing relationship will prevail when the computer again activates the output channel (Fig. 3.b). The synchronization process, therefore, occurs every time the computer activates the channel (every 2 seconds).

One result of this synchronization is that it is possible for the data to be as much as 50 ms in error in time. This is a negligible error. As the Haystack clock drifts slowly with respect to the West Ford clock, the instantaneous time error decreases slowly from maximum (50 ms) to zero, then jumps to maximum and starts to decrease again (or vice versa, depending on which clock is running at the higher rate), so that at least part of the time the system is synchronous (when the error is close to zero).

One additional feature of the system is the ability of the West Ford equipment to inform the 490 computer of the presence or absence of a target. This is accomplished by generating a double pulse on the 20-cps telephone line whenever a target is present. The data transmitter interprets this double pulse as a target indication and sends an external interrupt to the Haystack 490 computer on channel 12.

II. PLUG-IN CARDS

The intersite coupling link is constructed with three different types of plug-in cards. The interface uses Univac cards, the data transmitter uses Computer Control Company (3C) cards, and the data receiver uses Lincoln-built cards (the same cards used in the West Ford antenna pointing equipment).

Two types of Univac cards are used, an input amplifier and a control line driver. The Univac logic levels on the lines between the computer and the interface are:

"1" = 0 volts
"0" = -3 volts

The input amplifier is an inverter so that these logic levels are reversed at the output of the interface.

The 3C cards are organized around the "nand" circuit. Logic levels are:

"1" = -6 volts
"0" = 0 volts

The 3C D1-21 card is used to accept signals from the Univac input amplifier. This card accepts either -3 volts or -6 volts as a logic "one".

Detailed information on all 3C cards can be found in their "Instrumentation Manual, Publication No. 71-113A".

The Lincoln-built cards use "and-or" logic, and the logic levels are:

"1" = +5 volts

"0" = -5 volts

Schematics for all these cards, except for the modulator and demodulator (which are shown in Figs. 4 through 7), are available at the West Ford site.

III. DATA TRANSMITTER

A. Data Input (Figs. A-1 and A-2)

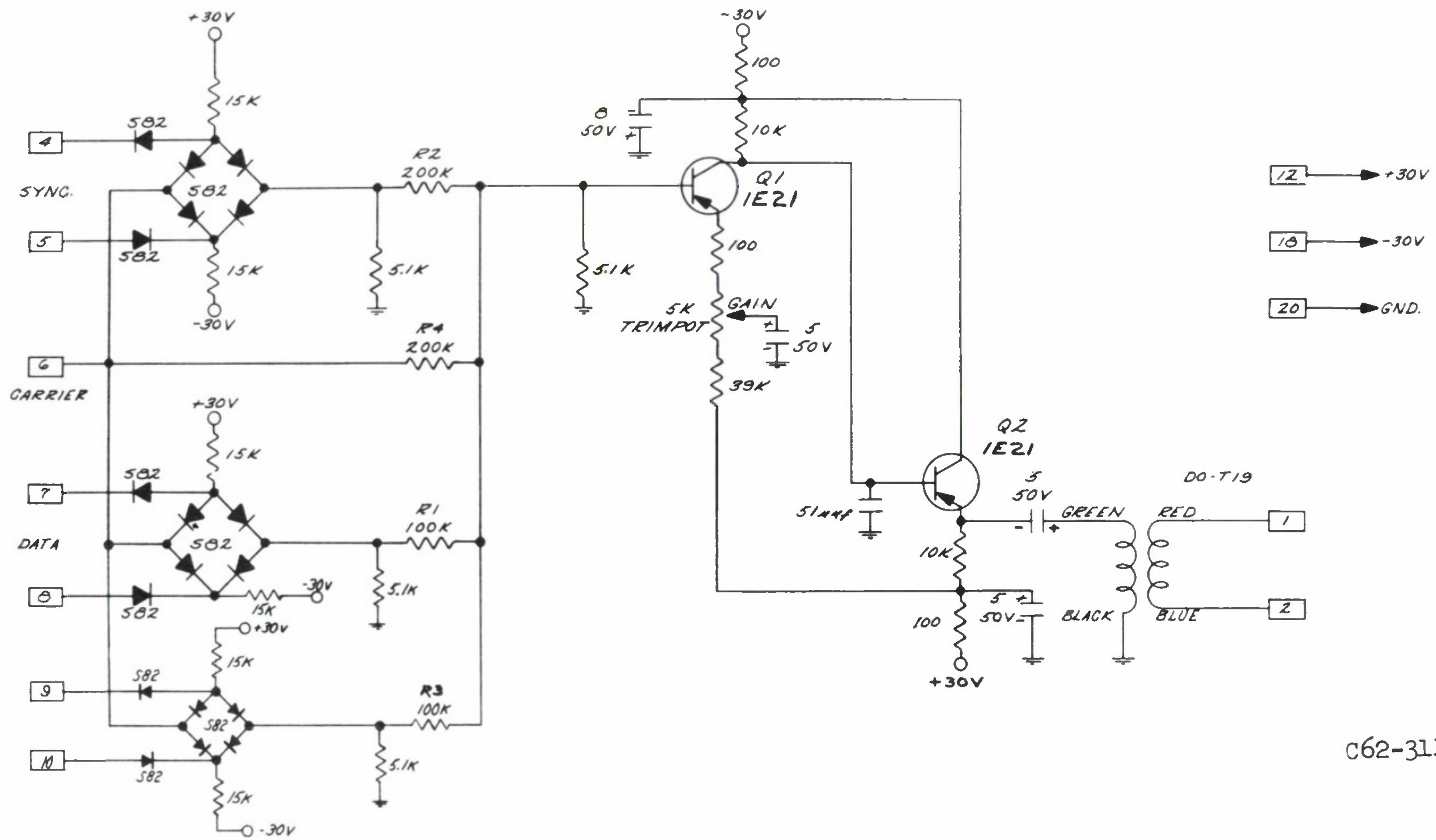
The thirty data lines from the 490 (channel 12) are connected to the data transmitter through jack J-1 which is connected to the OPERATE side of the TEST/OPERATE jacks J-3, J-4, J-5 and J-6. In the operate mode, pins 1-19, 2-20, etc., of J-5 and J-6 are shorted together; in the test mode, pins 1-19, 2-20, etc., of J-3 and J-4 are shorted together and the data source is the bank of test switches shown in the diagrams.

The outputs from the TEST/OPERATE jacks go to a set of Univac Input Amplifiers, the outputs of which are connected to a set of data gates. Set pulses (A-24-12, Fig. A-5) are also applied to these data gates, and whenever a particular data input is true (a logic one, or -3 volts), the set pulse is passed by the associated data gate and sets the associated flip-flop in the data transmitter shift register (Figs. A-3 and A-4).

The data gates for bits 28 and 29 have an extra input. This is used to inhibit these bits when the range word is loaded, which permits the transmitter to terminate transmission of the range word after bit 17 (bits 15 and 16 are used as the identity tag at the receiver).

This inhibit function is also used to prevent the set pulse from loading a dummy bit into the shift register through data gate A-4-7. This dummy bit is used to initiate end of transmission for the AZ/EL and doppler words, but bit 17 is used for this purpose for the range word.

Also in Fig. A-2, it is shown that in the test mode, bits 28 and 29 do not have test switches. These bits are simulated in order to permit the generation of a test message. The ACK signal is switched by the TEST/OPERATE jacks for the same reason.



+30V
15K
SB2
SYNC.
R2
200K
5.1K
-30V
R4
200K
CARRIER
DATA
R1
100K
R3
100K
-30V
100
10K
8
50V
Q1
1E21
5K
TRIMPOT
GAIN
39K
5
50V
Q2
1E21
51μμf
GREEN
BLACK
RED
BLUE
DO-T19
GND.

C62-311

Fig. 4

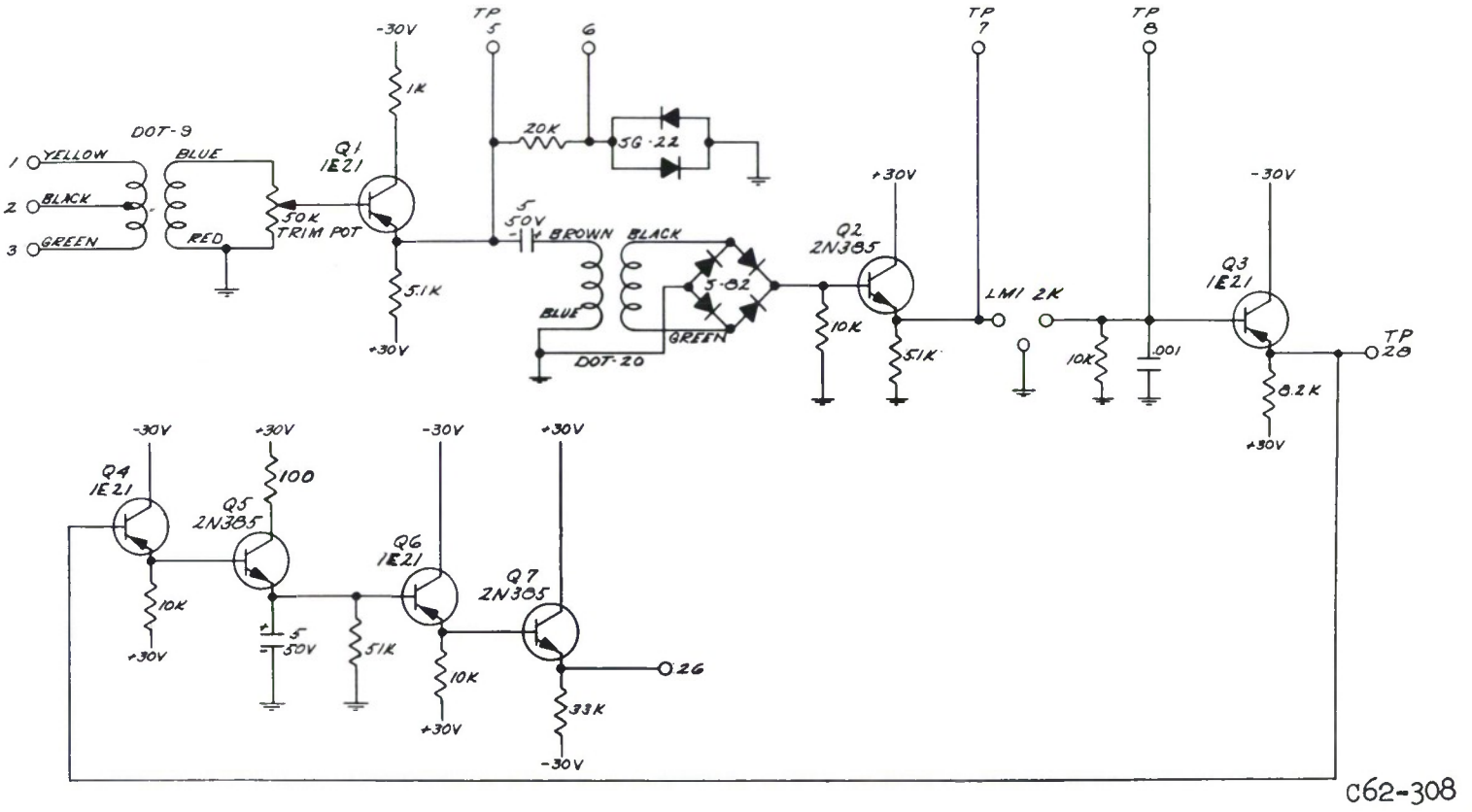

-30V
TP 5
6
TP 7
TP 8
1K
20K
5G-22
DOT-9
1 YELLOW
2 BLACK
3 GREEN
BLUE
RED
Q1 IE21
30K TRIM POT
5 50V
BROWN
BLACK
5-82
BLUE
GREEN
DOT-20
5.1K
+30V
Q2 2N385
10K
51K
LM1 2K
10K
.001
Q3 IE21
6.2K
TP 28
Q4 IE21
Q5 2N385
100
Q6 IE21
Q7 2N385
5 50V
51K
10K
33K
26
C62-308

Fig. 5

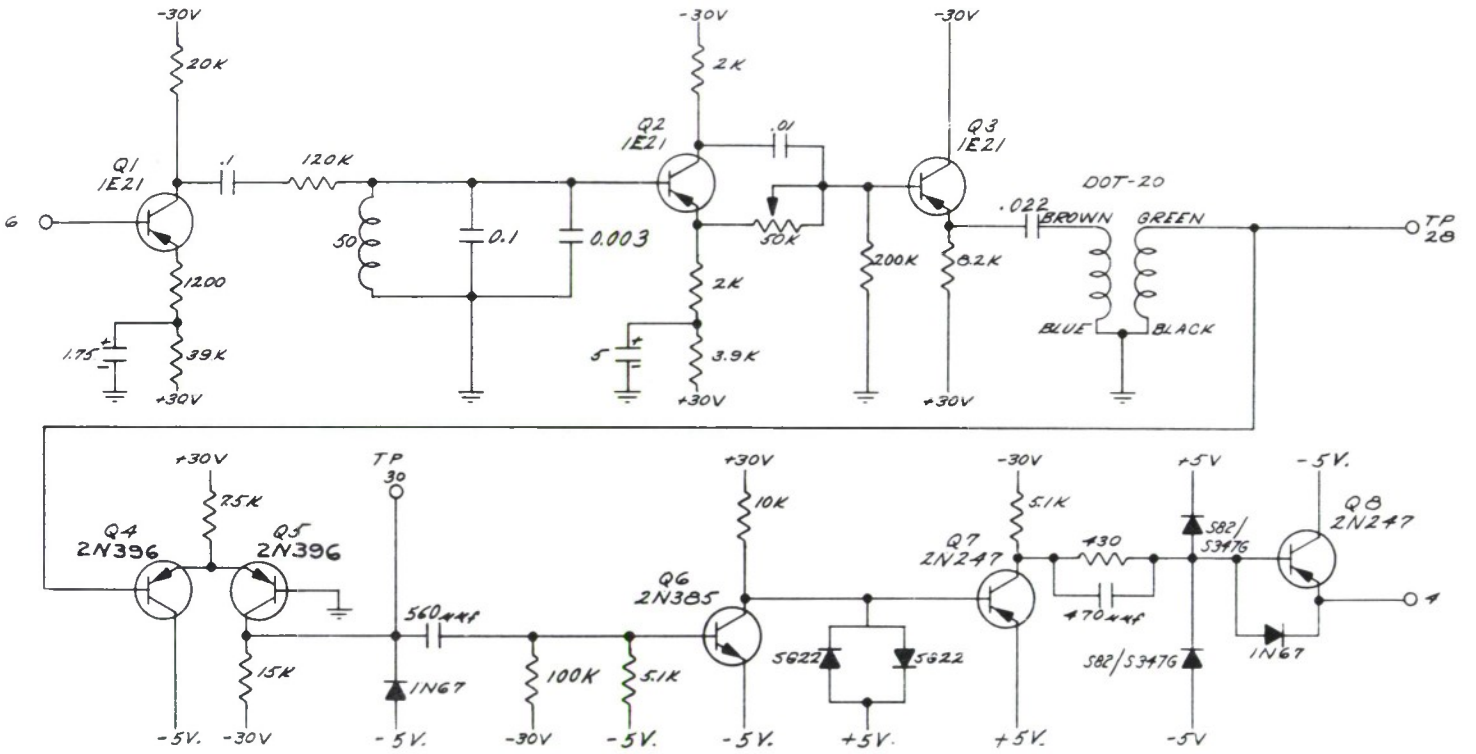

-30V
20K
Q1
1E21
.1
120K
G
1200
1.75
39K
+30V
50
0.1
0.003
-30V
2K
Q2
1E21
.01
50K
2K
5
3.9K
+30V
-30V
Q3
1E21
200K
8.2K
+30V
DOT-20
.022
BROWN
GREEN
BLUE
BLACK
TP
28
+30V
25K
Q4
2N396
Q5
2N396
15K
-5V.
-30V
TP
30
560μμf
1N67
-5V.
100K
-30V
5.1K
-5V.
+30V
10K
Q6
2N385
-5V.
5G22
5G22
+5V.
-30V
5.1K
Q7
2N247
+5V.
430
470μμf
+5V
S82/
S347G
S82/S347G
-5V
-5V.
Q8
2N247
1N67
4
C62-309

Fig. 6

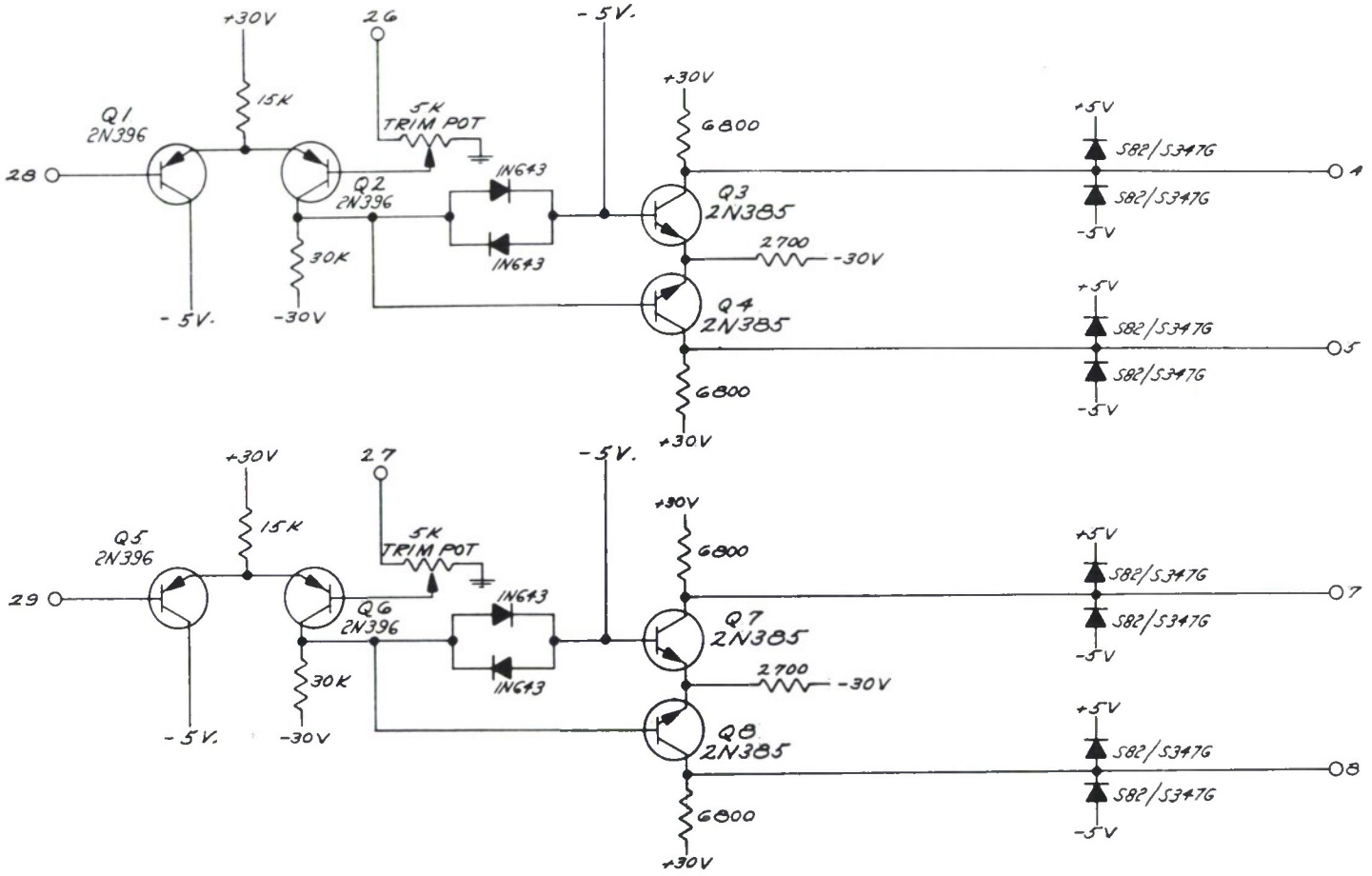

+30V
26
-5V.
15K
5K TRIM POT
Q1 2N396
28
Q2 2N396
1N643
1N643
30K
-5V.
-30V
+30V
6800
Q3 2N385
2700
-30V
Q4 2N385
6800
+30V
+5V
S82/S347G
S82/S347G
-5V
1
5
+30V
27
-5V.
15K
5K TRIM POT
Q5 2N396
29
Q6 2N396
1N643
1N643
30K
-5V.
-30V
+30V
6800
Q7 2N385
2700
-30V
Q8 2N385
6800
+30V
+5V
S82/S347G
S82/S347G
-5V
7
8
C62-310

Fig. 7

B. Shift Register (Figs. A-3 and A-4)

The diagrams show the 32-stage register used in the transmitter. The dummy bit from A-4-7 is loaded into the first stage (A-2-28), the 30 data bits are loaded into the next 30 stages, and nothing is loaded into the last stage which serves as a one clock delay during shifting.

The register is cleared via A-26-6, 7 (Fig. A-3) and A-26-12, 16 (Fig. A-4) whenever the ODR flip-flop (A-20-7, Fig. A-6) is set.

Shift clocks are applied to the registers via the buffers at the top of the diagrams, and the logic beneath the shift register comprises one large matrix which senses for the condition when all stages of the shift register, except the final one, are clear. This condition is defined as end of transmission, which always occurs when the dummy bit (or bit 17 for the range word) arrives at the final stage.

C. 20-Cps, INTERRUPT and SET Logic (Fig. A-5)

The 20-cps signal from West Ford is sliced by slicer A-23-27, the output of which sets flip-flop A-28-28. This flip-flop is then cleared by the next 2-Kc clock, and its output is used to set flip-flops A-20-12 (bit 29 check) and A-28-12 (interrupt enable).

The next 2-Kc clock clears A-28-12. If a second pulse (indicating the presence of a target at West Ford) occurs on the 20-cps phone line, the slicer output from this second pulse sets the interrupt flip-flop (A-28-7); this slicer output cannot reset flip-flop A-28-28 because A-28-12 inhibits the input to A-28-28 at this time.

If the interrupt enable switch (front panel) is on, the computer will sense the interrupt and generate an input acknowledge signal which fires one-shot A-22-10, which then clears the interrupt flip-flop. If, for some reason, the computer did not acknowledge the interrupt or if the interrupt enable switch were off, the next 20-cps signal clears the interrupt flip-flop.

The bit 29 check flip-flop is used to ensure that an AZ/EL word is sent from the computer in response to an ODR generated by a 20-cps signal. When the computer generates an output acknowledge in response to an ODR, the matrix A-24-12 determines whether or not a set pulse will be generated. If the bit 29 check flip-flop is set and if data bit 29 is false (a logic zero, or 0 volts), then the matrix passes the acknowledge signal thus generating a set signal which loads the data and clears the bit 29 check flip-flop.

D. ODR Logic (Fig. A-6)

The ODR flip-flop A-20-7 is set by any one of three sources:

1. 20-Cps signal (flip-flop A-28-28) via matrix A-18-6, matrix A-24-16.
2. ΔEOT (matrix A-24-23) via the same route.
3. Repeat (flip-flop A-21-11) via matrix A-24-16.

In all cases, the ODR flip-flop is cleared by the output acknowledge generated by the computer via the one-shot A-22-28 (except in the test mode, in which case the acknowledge is generated by matrix A-18-12). In addition, the ODR flip-flop may be cleared manually by means of a front panel switch.

The 20-cps signal (essentially) unconditionally sets the ODR flip-flop. The ΔEOT signal is the delayed (by 2 clocks) end of transmission signal which sets the ODR flip-flop after transmission of the previous word is completed. The ΔEOT counter, flip-flops A-20-27 and A-20-30, counts ΔEOT signals and prevents the ΔEOT signal which occurs at the end of transmission of the range word from setting the ODR.

The repeat flip-flop is set by the output acknowledge signal whenever matrix A-24-33 prevents the acknowledge from generating a set pulse. The repeat flip-flop is then cleared by the next 2-Kc clock, and its output sets the ODR flip-flop. This process continues until matrix A-24-33 is satisfied (i.e., when an AZ/EL word is transferred).

The guard flip-flop (A-28-30) is set whenever the ODR flip-flop is set and is then cleared by the output acknowledge signal. This flip-flop guarantees that the ODR flip-flop, once cleared, will not be set again for at least 10 μs (the width of the ACK one-shot). This is a requirement of the U-490 logic. *

E. Data, Parity and the P/L Modulator (Fig. A-7)

The data shift register supplies data to the data flip-flop (A-19-31) via matrix A-17-33; when end of transmission occurs, this matrix supplies the parity bit (flip-flop A-19-28) to the data flip-flop. The parity flip-flop commutates on data; if there are an even number of "ones" in the data, the parity flip-flop is in its original (clear) state at end of transmission time, and a zero is sent to the data flip-flop as the parity bit. If there are an odd number of "ones" in the data, the parity flip-flop is in

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*See Univac Service Manual PX2122, pp. 4-260 and 4-271.

the set state at end of transmission time, and a "one" is sent to the data flip-flop as the parity bit. The result is that each data word always contains an even number of "ones".

The data flip-flop outputs drive the phone line modulator (A-27, see also Fig. A-9) which amplitude modulates a 2-Kc timing signal with sync and data; the ratio of sync to data to timing is 4:2:1, with the sync amplitude set at 2.2 volts peak to peak.

F. ΔEOT Logic (Fig. A-7)

Flip-flops A-19-7 and A-19-12 comprise a two-stage shift register which serves to delay the end of transmission signal for two clock intervals. The delayed output goes to the matrix shown in the diagram. This matrix allows the delayed EOT signal to gate one clock pulse which is used to advance the ΔEOT counter, set the ODR flip-flop, and clear the data gate flip-flop. The prime side of the 20-cps flip-flop (A-28-27) inhibits this matrix when the 20-cps signal occurs; this is done to prevent the ΔEOT counter from advancing to an incorrect count.

G. Clock Generation (Fig. A-7)

The clock generation circuitry consists of a 2-Kc tuning fork oscillator, a slicer and a one-shot. The sine wave output from the tuning fork (which is used as the phone line carrier) is sliced by A-23-10, and this output fires one-shot A-22-6 which provides clock signals wherever needed.

H. Sync and Data Gate (Fig. A-7)

Flip-flops A-21-27 and A-21-30 comprise a standard two-flip-flop phasing circuit. The set pulse, generated by the output acknowledge pulse from the computer, sets the pre-sync flip-flop; this permits the next clock pulse to set the sync flip-flop, and this action clears the pre-sync flip-flop. The next clock then clears the sync flip-flop, the output of which goes to the phone line modulator.

The same clock that clears the sync flip-flop also sets the data gate flip-flop (A-21-6). The output of this flip-flop gates clock pulses through the matrix in A-25 which provides gated shift clocks for the shift register.

The data gate is cleared whenever the ODR is set by buffer A-25-16.

I. Test Mode

When the TEST/OPERATE jacks are connected for test, the switch bank in Figs. 1 and 2 provides data inputs for bits 0 through 27, and bits 28 and 29 are

simulated by flip-flops A-20-31 (Fig. A-6) and A-20-12 (Fig. A-5), respectively.

Flip-flop A-20-12 (simulating bit 29) is set by the 20-cps signal so that its "one" output is at -6 v (logic one). The "zero" side of this flip-flop is inverted by A-25-23 (Fig. A-5), and this output goes to the input amplifier B-15-13 (Fig. A-2). This signal is at -6 v which is the correct level for a logic "zero" at the input to this amplifier.

Flip-flop A-20-31 (simulating bit 28) is cleared by the 20-cps slicer output to -6 volts. This level goes to input amplifier B-15-12 (Fig. A-2) and also represents a logic "zero".

The ODR flip-flop A-20-7 (Fig. A-6) is also set by the 20-cps signal, and its output gates a clock pulse through matrix A-26-23 (Fig. A-6). The output of this matrix goes through the TEST/OPERATE jack and fires the acknowledge one-shot A-22-17 (Fig. A-6).

Since the bit 29 check flip-flop is set and since the simulated bit 29 is a zero, the matrix in A-24-12 will generate a set pulse which clears the bit 29 check flip-flop and loads whatever data bits are set on the test switches into the shift register.

With the bit 29 check flip-flop cleared, the simulated bit 29 becomes a "one", and it remains in that state until the next 20-cps signal.

After the transmitter has sent the first word out, a ΔEOT signal occurs, a new ODR is generated, and the ΔEOT counter is advanced. The ODR again acknowledges itself, and the second word is loaded into the shift register and transmitted (simulated bit 29 is a "one", simulated bit 28 is still "zero").

After this second word is sent, another ΔEOT signal occurs which generates another ODR and advances the ΔEOT counter. This causes the simulated bit 28 to change state so that when the third word is loaded into the shift register, both simulated bits are "ones".

The bank of test switches provides data for all three words, and in order to generate a correct range word, it is necessary to have switches 15, 16, and 17 in the one state and to have no higher order switches in the one state. With this limitation, the test switches can be used to send all possible range, azimuth and monostatic doppler words; the least significant three bits of elevation are always present, and the bistatic word is nonsense.

IV. DATA RECEIVER

A. Demodulator (Fig. B-1)

The demodulator consists of the three cards located in III. K-3, III. H-3, and III. H-4. The phone line signal is supplied to the demodulator I card in III. H-3 where the signal is full wave rectified and filtered and also limited.

The rectified signal appears on pin 28, and the limited signal appears on pin 6. The latter signal is supplied to the demodulator II card in III. H-3 which contains a ringing circuit tuned to 2 Kc. The sine wave out of the ringing circuit goes through a phase shifter and then to a differentiator and clipper which delivers narrow clock pulses. The phase shifter is used to position these clock pulses relative to the demodulated data.

The rectified signal from the demodulator I card is supplied to the demodulator III. card which is essentially two slicers. One slicer is set to detect only sync pulses, and the other is set to pass both data "ones" and sync.

B. Sync, Data Gate, and Parity (Fig. B-1)

The detected sync from III. H-4-4 goes to BIMI III. H-5-1 where it is "anded" with clock. The output of this BIMI then is a clock pulse that occurs only at sync time. It fires one-shot III. H-2-21, the output of which is used to clear the receiver shift register (Figs. B-3, B-4), the parity flip-flop and the data gate. The BIMI output (III. H-5-1) also sets the Δ sync flip-flop (III. H-7-1) which is cleared by the next clock; this same clock sets the data gate enable flip-flop (III. H-7-21) which is cleared by the subsequent clock. This clock also sets the data gate flip-flop (III. H-8-1) which gates the clock in BIMI III. H-5-21. This gated clock is used as the shift clock in the receiver shift register and in the parity flip-flop.

The parity flip-flop is initially set to the one state by sync and it then commutates on shifted data. If there are an even number of "ones" in the word, the flip-flop will end up in the one state after the word has been shifted in.

The data gate is cleared when the shift register is full by the end of transmission signal (EOT).

C. Transfer Logic (Fig. B-2)

After a complete word has been shifted into the data receiver, an end of transmission (EOT) signal occurs. This signal triggers one-shot III. H-2-1 which in turn sets the transfer flip-flop III. H-8-21, provided that no sync pulse is present. This

provision is included to prevent erroneous data transfers when the data transmitter at Haystack is going through its synchronization process.

The output of the transfer flip-flop goes to pin 7 of the transfer matrix III. K-6. The top section of this matrix passes the transfer pulse if parity is correct, the word tag is correct (AZ/EL word, bit 29 a "zero"), EOT is true, and the function JG' is true. This last function is generated in the arithmetic section of the West Ford pointing equipment, and it is true so long as no arithmetic is in progress. The transfer pulse passed by this matrix is sent via pulse shaper III. K-7-21 and BIMI IV. B-1-1 (Fig. B-5) to the AZ/EL clear and set logic (see page IV. 4 of the logic diagrams for the West Ford pointing equipment). As a result, the AZ/EL word in the data receiver is transferred via the switching relay (Fig. B-6) to the AZ/EL command registers in the pointing equipment.

The middle section of the transfer matrix passes the transfer pulse if parity is correct, if the identity tag is correct (doppler word, bit 29 a "one", bit 28 a "zero"), and EOT is true. The transfer pulse passed by this matrix is sent via pulse shaper III. K-7-22 to one-shot II. H-4-1 (Fig. B-5). This one-shot is triggered repetitively by a 50-Kc clock so long as the transfer pulse is true, thus generating a train of read pulses which loads the doppler word from the data receiver into the doppler display register in the pointing equipment.

The bottom section of the transfer matrix passes a 20-cps signal if parity is correct, the identity tag is correct (range word, bits 28 and 29 both "ones") and EOT is true. This 20-cps signal is sent via pulse shaper III. K-7-23 and BIMI IV. B-1-21 (Fig. B-5) to the range clear and set logic (see page III-2 of the logic diagrams for the West Ford pointing equipment). As a result, the range word in the data receiver is transferred via the switching relay (Fig. B-6) to the range command register in the pointing equipment.

D. 20-Cps Logic (Fig. B-2)

Flip-flops III. K-8-1 and III. K-8-21 comprise a standard two-flip-flop phasing circuit which phases the West Ford 20-cps signal with the intersite 2-Kc clock. The phased output drives a phone line modulator which generates a dipulse (one cycle of the 2-Kc sine wave from the demodulator II card, Fig. B-1) which is sent to the data transmitter at Haystack over the second telephone line.

The target indicator flip-flop III. K-4-30 is normally clear and does not interfere with operation of the phasing circuit. At some future date, the slicer indicated in the

diagram will be added to the system and whenever a target is detected, its output will set the target indicator flip-flop. When the next 20-cps signal occurs, the phasing circuit will then put out a double dipulse on the phone line and will clear the target indicator flip-flop. This double pulse on the telephone line is interpreted by the data transmitter as indicating the presence of a target, and the computer at Haystack is so informed by means of an interrupt.

E. Dummy Bit Logic (Fig. B-2)

The dummy bit flip-flop III. K-5-21 is cleared by the phased 20-cps or by sync. The outputs from this flip-flop are loaded into the first stage and the fourteenth stage of the receiver shift register (Fig. B-3). When the flip-flop is in the clear state, a "one" is loaded into the first shift register stage and a zero into the fourteenth stage by the sync pulse.

The doppler transfer pulse sets the dummy bit flip-flop to the "one" state, provided that the guard flip-flop III. K-4-10 is clear, and the next sync pulse (which heralds the arrival of a range word) loads a "zero" into the first shift register stage, and a "one" into the fourteenth stage

The bit loaded into the shift register by the dummy bit flip-flop propagates down the register along with data and when it arrives at the last stage in the register, an EOT signal occurs which clears the data gate and terminates the shift clock. Therefore, the AZ/EL and doppler words are shifted the full length of the register (31 clocks) while the shorter range word is only shifted part way (18 clocks).

The guard flip-flop is set by the 20-cps signal and cleared by sync. This flip-flop prevents the dummy bit flip-flop from being set should a 20-cps signal occur close to the time that the doppler transfer pulse occurs (this can happen when the data transmitter is going through its synchronization process).

F. Shift Register (Figs. B-3 and B-4)

Eight SR-4 cards in slots III. H-11 through III. H-18 comprise the 32-stage receiver shift register. Data from the telephone line is entered serially into the register until it is fully loaded at which time a parallel data transfer occurs. AZ/EL data are taken from the "one" outputs of the register through 2K isolating resistors. Range and Doppler data are taken from the "zero" outputs through gating matrices.

These matrices are "or" gates and the gating level which comes from the mode switch (Fig. B-7) via BIM2 III. K-21-9 (Fig. B-4) is at -5 v (logic zero) in the intersite

mode. This permits the shift register data to be sent to the set of BIM2's shown beneath the matrices in the diagrams, and the outputs of these BIM2's drive cables which supply the data to the doppler display register and, via the switching relay, to the range command register.

The notation within the SR-4 blocks on the diagrams shows the position in the shift register of each AZ/EL data bit and each doppler bit during the parallel data transfer. The notation within the BIM2 blocks shows the position of the range bits.

When the mode switch is in the paper tape position, the gating level to the matrices is at +5 v (logic one) which forces the outputs of the matrices to +5 v regardless of the data in the shift register. This causes the outputs of the BIM2's to present data "zeroes" to the doppler display register inputs, as this is required for paper tape operation (in this mode, the doppler display register is cleared by reading in "zeroes" in parallel and then loaded serially with data from the paper tape).

G. Transfer Logic Modifications (Fig. B-5)

This diagram shows the modifications made to the logic of the West Ford pointing equipment to permit intersite coupling operation. The original transfer signal for the AZ/EL word goes from III. J-13 to IV. C-14-2 (see page IV-4*); the same signal goes to III. C-19-8 (page III-2) to transfer the range word.

For intersite coupling, a BIMI has been added in slot IV. B-1 to switch the transfer pulse. In paper tape operation, as determined by the mode switch, the normal transfer function is sent from IV. B-1-1 to IV. C-14-2 for AZ/EL and from IV. B-1-21 to III. C-19-8 for range. In the intersite mode, the matrices at the input to the BIMI select the transfer functions from the intersite transfer matrix (Fig. B-2) in lieu of the normal transfer signal.

For the Doppler word, the one-shot II. H-4-1 (page II-5) normally clears the doppler display register. In the intersite coupling mode, this one-shot is used to transfer the Doppler word from the receiver shift register to the display register. To this end, the matrix at the input to this one-shot was enlarged. In the paper tape mode, as determined by the mode switch, the one-shot works normally, generating

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*The page references in this section refer to pages in the logic diagrams of the West Ford pointing equipment.

a train of clear pulses when an A-block is loaded. In the intersite mode, the one-shot matrix accepts the doppler transfer pulse from the receiver transfer logic (Fig. B-2) and generates a short train of set pulses at this time.

The Doppler sign bits required the addition of the BIMI's in II. H-1 and II. H-2. The matrices on the inputs to these cards permit normal operation in the paper tape mode and modified operation in the intersite mode (see pages II-12 and II-13 for the original logic).

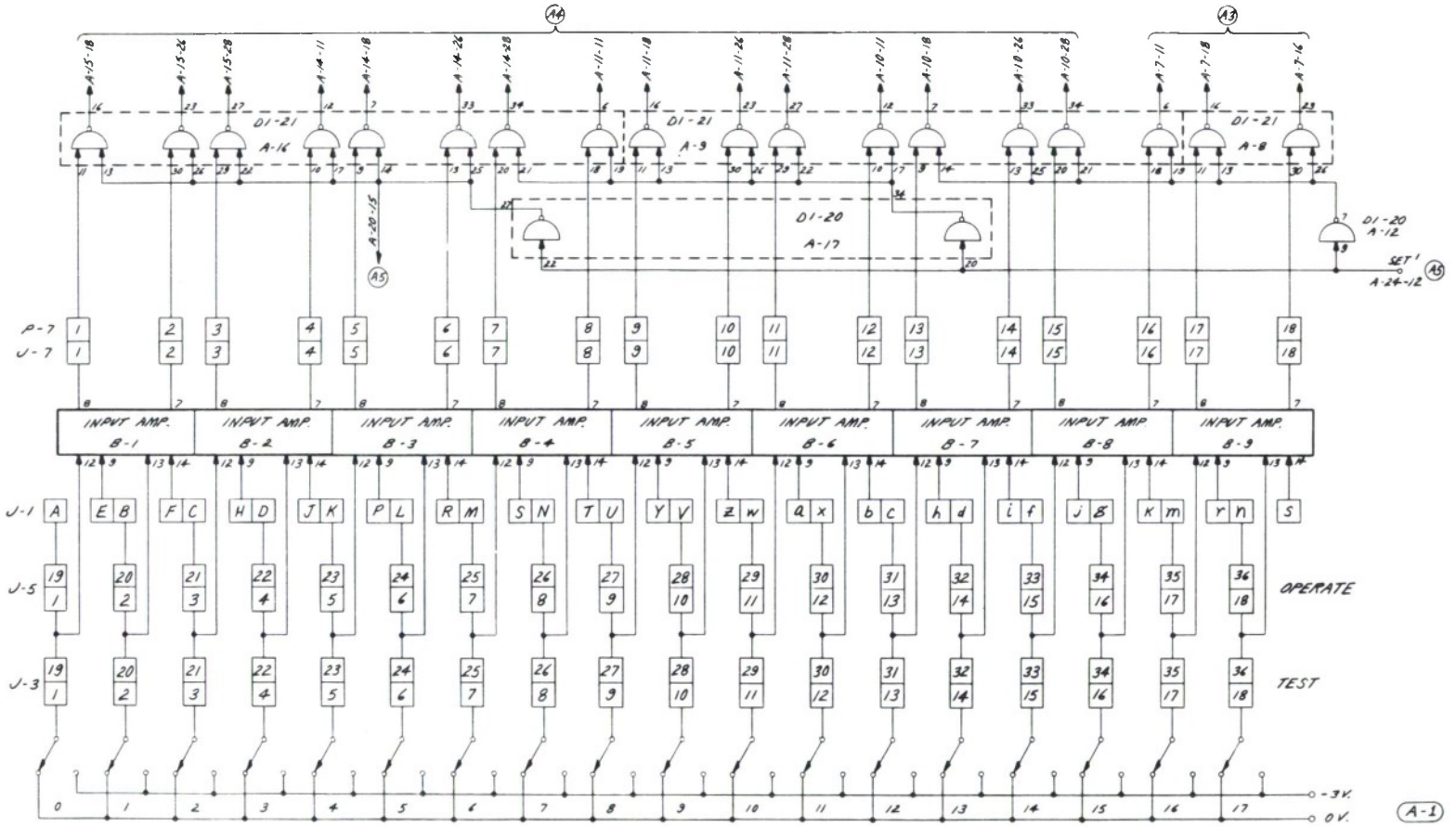
H. Switching Relay (Fig. B-6)

The relay shown in the diagram switches the inputs to the AZ/EL and range command registers between the normal source (the storage registers in the paper tape reader logic) and the intersite coupling source (the data receiver shift register). For simplicity, all relay contacts are not shown; the relay physically consists of two multipole relays, and 32 poles of each relay are used. Pin 1 of XJ-35 goes to a normally closed (NC) contact; the associated pole (C) is tied to Pin 1 of XP-35, and the normally open (NO) contact goes to Pin 1 of XJ-1. This connection scheme holds for all pin numbers so that the relay switches the input to XP-35 between XJ-35 and XJ-1 and the input to XP-34 between XJ-34 and XJ-2.

Range and Azimuth data from the paper tape storage appear on III. P-35 and in the paper tape mode, this plug is connected via the relay to III. J-35. Range and Azimuth data from the intersite coupling data receiver appear on XP-1 and in the intersite coupling mode, this plug is connected via the relay to III. J-35 which connects the data to the input to the Azimuth and Range command registers of the pointing equipment (see pages III-1 and IV-2 of the logic for the West Ford pointing equipment).

The Elevation data is similarly switched by the second section of the relay.

JEG:pm



C62-312

Fig. A-1

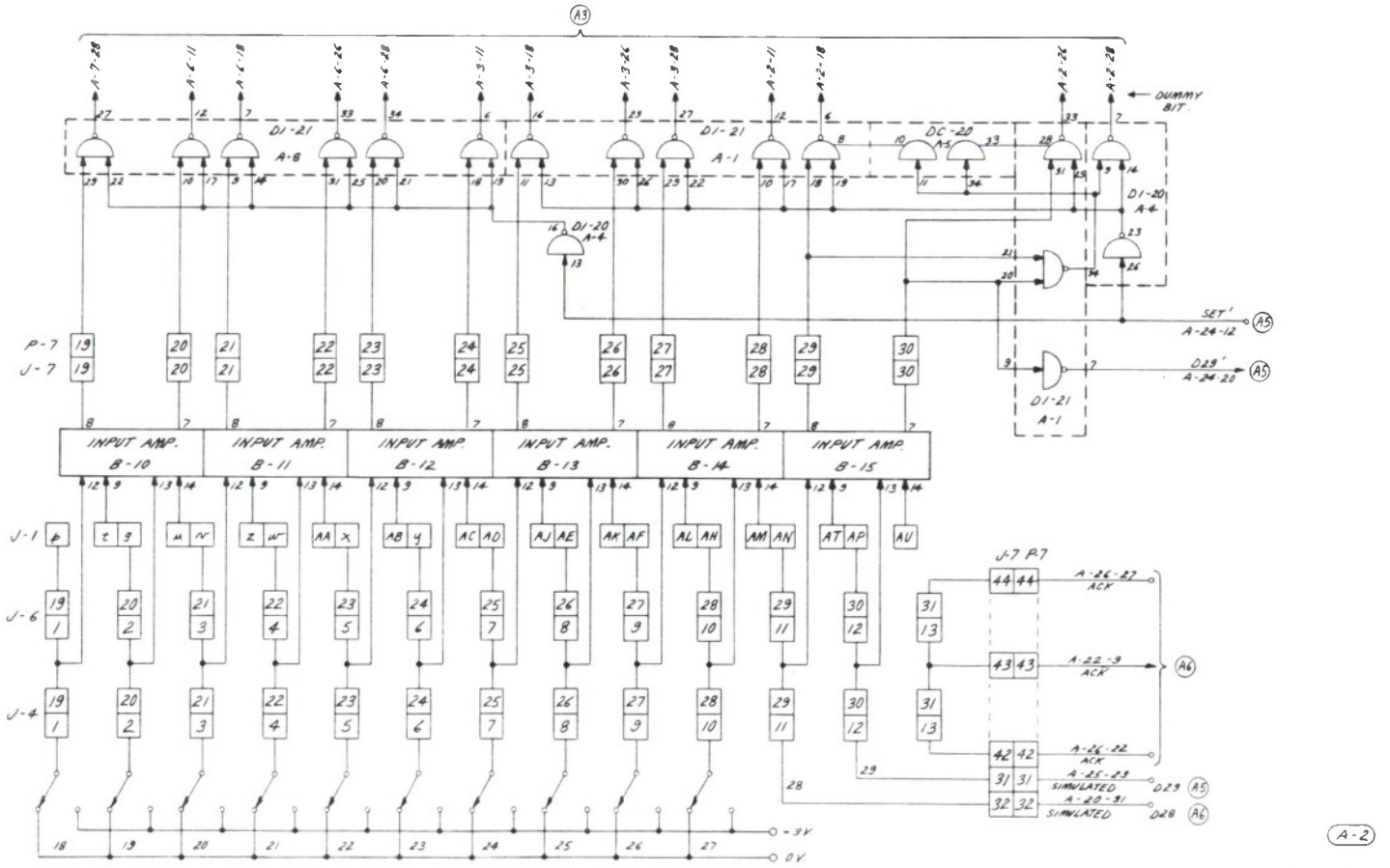

A3
DUMMY BIT
DI-21 A-8
DI-21 A-1
DC-20 A-5
DI-20 A-4
DI-21 A-1
SET' A-24-12
D29' A-24-20
INPUT AMP. B-10
INPUT AMP. B-11
INPUT AMP. B-12
INPUT AMP. B-13
INPUT AMP. B-14
INPUT AMP. B-15
P-7
J-7
J-6
J-4
J-1
J-7 P7
A-26-27 ACK
A-22-9 ACK
A-26-22 ACK
A-25-23 SIMULATED
A-20-31 SIMULATED
D29
D28
-3V
0V
A-2
C62-313

Fig. A-2

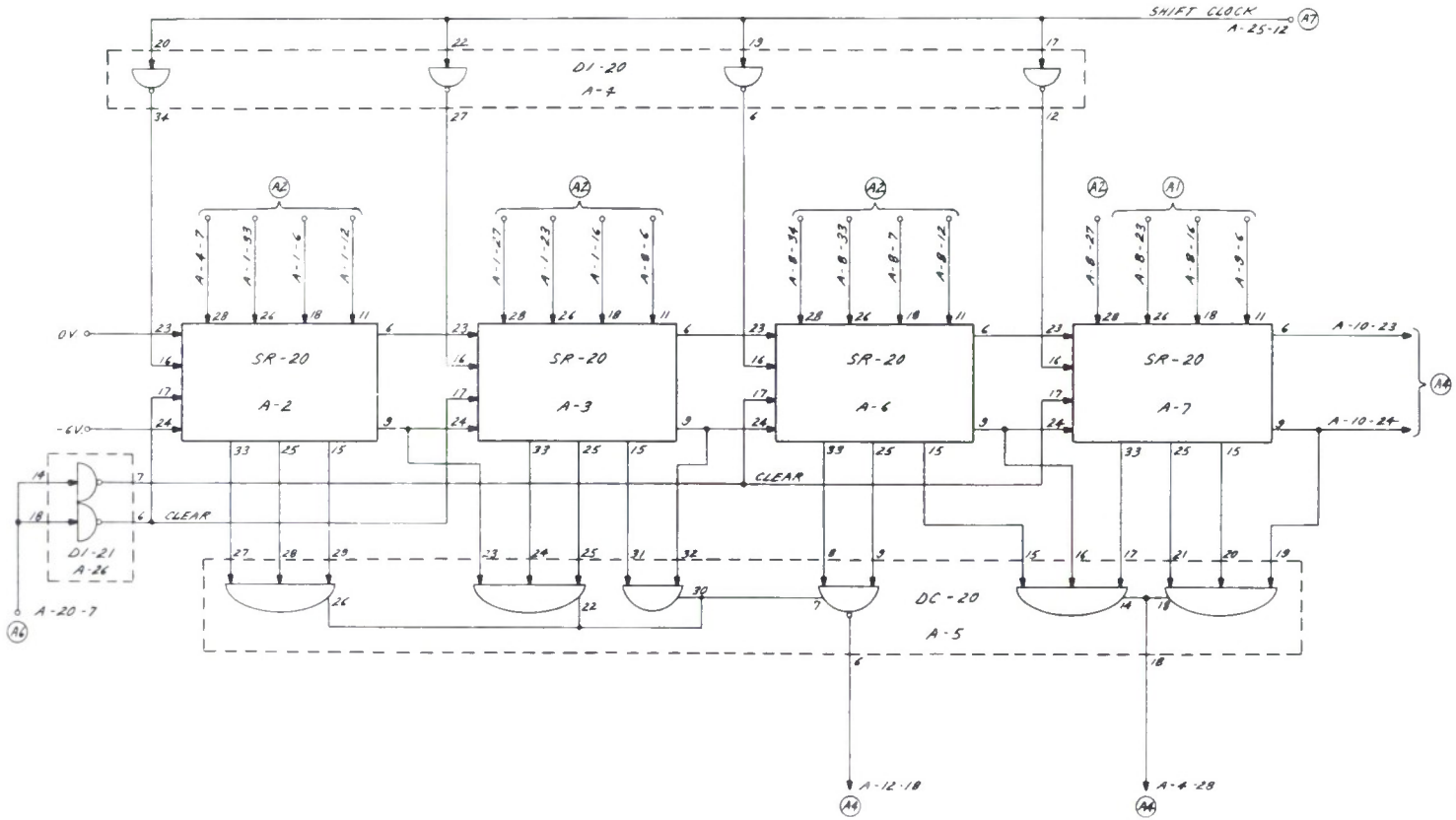

SHIFT CLOCK
A-25-12
A7
DI-20
A-7
SR-20
A-2
SR-20
A-3
SR-20
A-6
SR-20
A-7
0V
-6V
CLEAR
DI-21
A-26
A-20-7
A6
DC-20
A-5
A-10-23
A-10-24
A4
A-12-18
A-4-28
A-3
C62-314

Fig. A-3

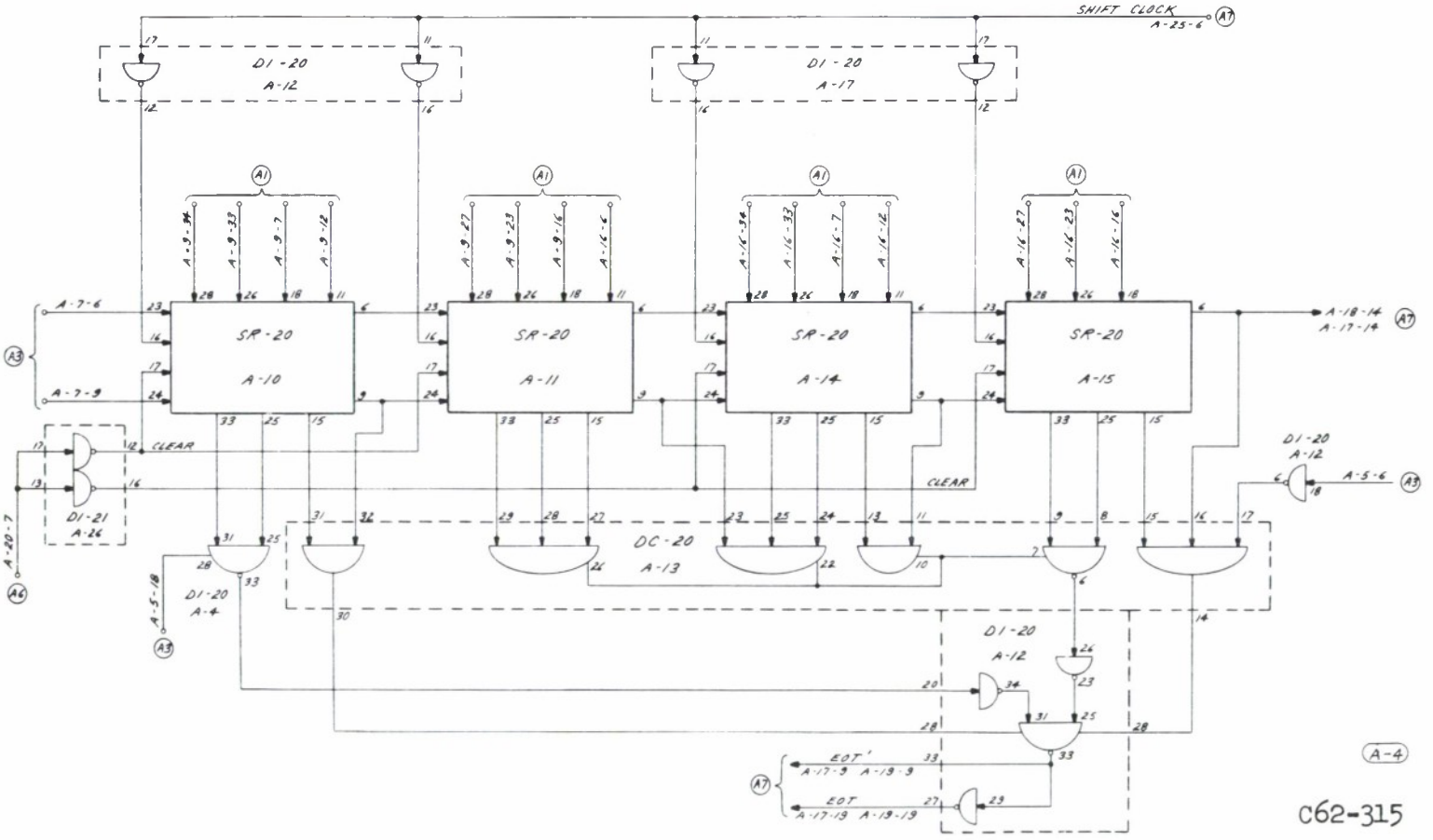
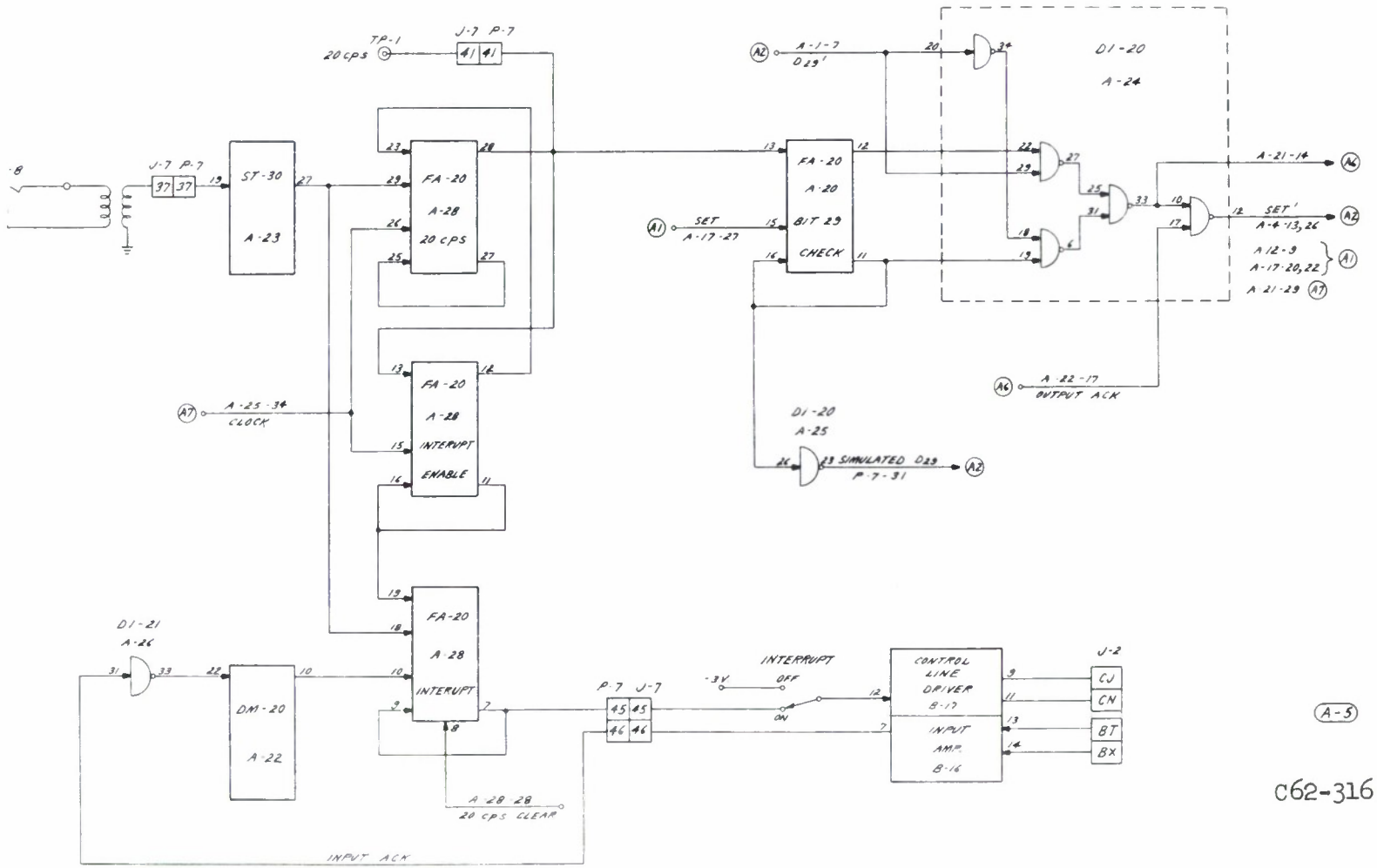

SHIFT CLOCK
A-25-6
DI-20
A-12
DI-20
A-17
SR-20
A-10
SR-20
A-11
SR-20
A-14
SR-20
A-15
A-7-6
A-7-9
CLEAR
DI-21
A-26
DC-20
A-13
DI-20
A-4
DI-20
A-12
A-18-14
A-17-14
A-5-6
EOT'
A-17-9 A-19-9
EOT
A-17-19 A-19-19
A-4
C62-315

Fig. A-4



C62-316

Fig. A-5

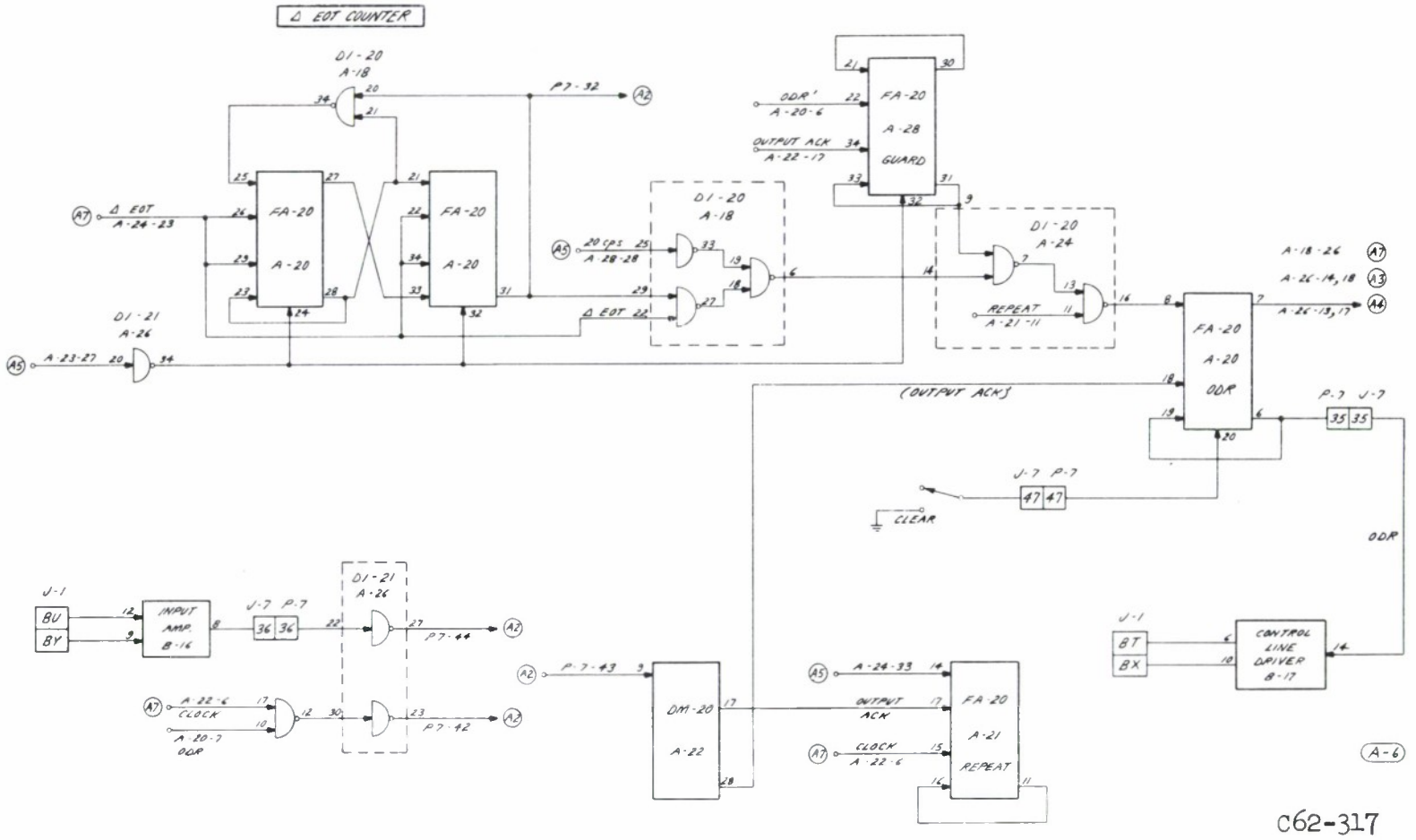

Δ EOT COUNTER
DI-20 A-18
P.7-32
FA-20 A-20
Δ EOT A-24-23
FA-20 A-20
20 CPS A-28-28
DI-20 A-18
Δ EOT 22
ODR' A-20-6
OUTPUT ACK A-22-17
FA-20 A-28 GUARD
DI-20 A-24
REPEAT A-21-11
A-18-26
A-26-14,18
A-26-13,17
DI-21 A-26
A-23-27
(OUTPUT ACK)
FA-20 A-20 ODR
P.7 J.7
35 35
J-7 P-7
47 47
CLEAR
ODR
J-1
BU
BY
INPUT AMP B-16
J-7 P-7
36 36
DI-21 A-26
P.7-44
A-22-6 CLOCK
A-20-7 ODR
P.7-42
P-7-43
DM-20 A-22
A-24-33
OUTPUT ACK
CLOCK A-22-6
FA-20 A-21 REPEAT
J-1
BT
BX
CONTROL LINE DRIVER B-17
A-6
C62-317

Fig. A-6

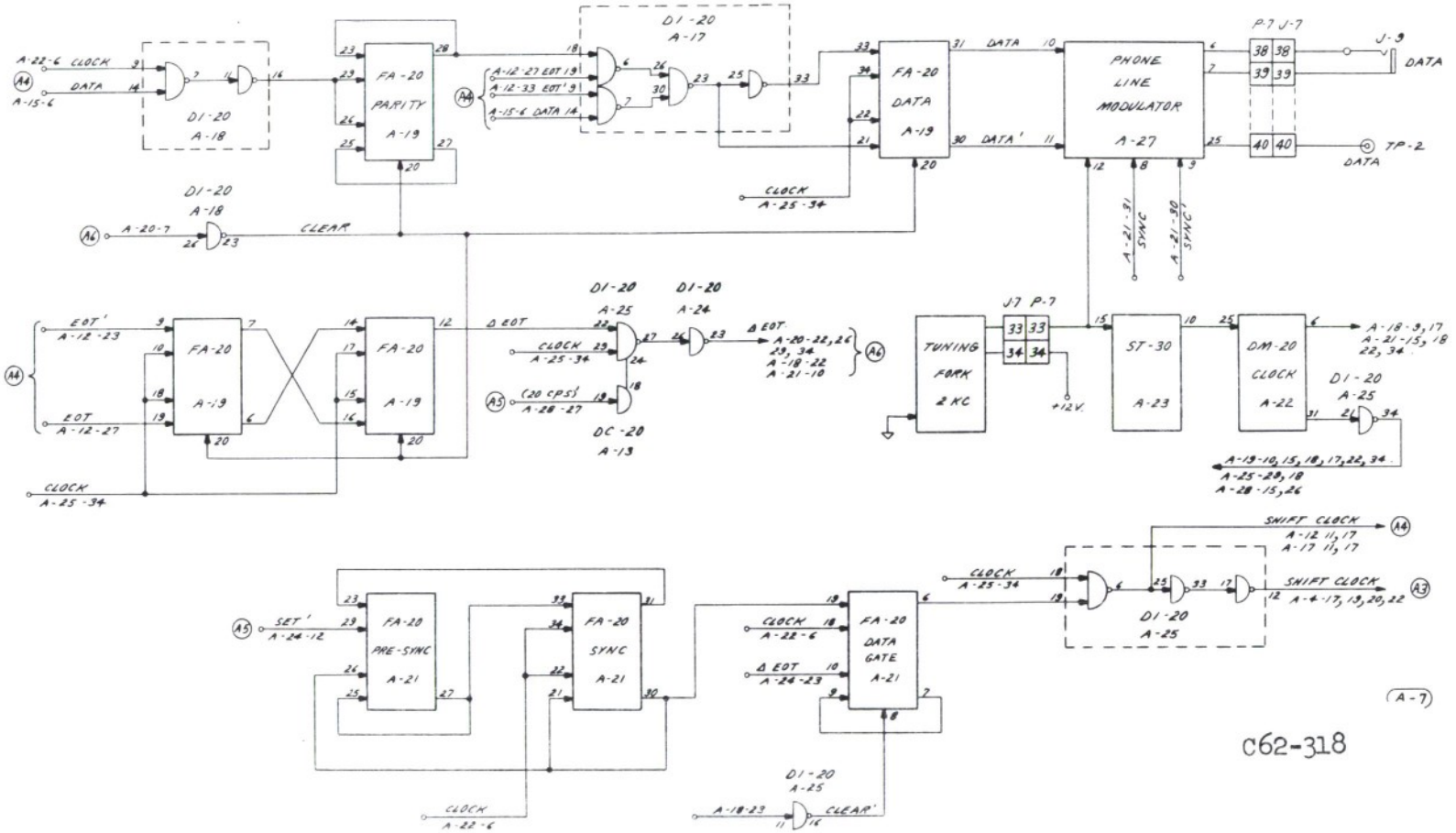

A-22-6 CLOCK
DATA
A-15-6
D1-20
A-18
FA-20
PARITY
A-19
D1-20
A-17
A-12-27 EOT 19
A-12-33 EOT' 9
A-15-6 DATA 14
FA-20
DATA
A-19
DATA
DATA'
PHONE
LINE
MODULATOR
A-27
P-7 J-7
J-9
DATA
TP-2
DATA
CLOCK
A-25-34
A-21-31
SYNC
A-21-30
SYNC'
A-20-7
CLEAR
EOT'
A-12-23
EOT
A-12-27
FA-20
A-19
FA-20
A-19
Δ EOT
D1-20
A-25
D1-20
A-24
CLOCK
A-25-34
(20 CPS)
A-28-27
DC-20
A-13
A-20-22, 26
29, 34
A-18-22
A-21-10
TUNING
FORK
2 KC
+12V.
J-7 P-7
ST-30
A-23
DM-20
CLOCK
A-22
A-18-9, 17
A-21-15, 18
22, 34
D1-20
A-25
A-19-10, 15, 18, 17, 22, 34
A-25-29, 18
A-28-15, 26
SHIFT CLOCK
A-12 11, 17
A-17 11, 17
CLOCK
A-25-34
D1-20
A-25
SHIFT CLOCK
A-4-17, 19, 20, 22
SET'
A-24-12
FA-20
PRE-SYNC
A-21
FA-20
SYNC
A-21
CLOCK
A-22-6
Δ EOT
A-24-23
FA-20
DATA
GATE
A-21
D1-20
A-25
A-18-23
CLEAR'
CLOCK
A-22-6
A-7
C62-318

Fig. A-7

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DUMMY	EOT	D_{26}	SHIFT	EOT	D_{22}	D_{18}	$\overline{22}$	$\overline{14}$	D_{14}	D_{10}	EOT	EOT	D_6	D_2	$\overline{6}$	SET	Δ EOT	PARITY	ODR	PRE SYNC	OUT ACK	20 ~	SET	CLOCK	CLR 20		20 CPS
$\overline{26}$			SHIFT	INHIBIT $\overline{28}$			$\overline{18}$	$\overline{10}$			EOT	EOT			$\overline{2}$	SET	ODR						SET	Δ EOT	OUT ACK		
$\overline{28}$	D_{29}	D_{25}	SHIFT	EOT	D_{21}	D_{17}	$\overline{23}$	$\overline{15}$	D_{13}	D_9	EOT	EOT	D_5	D_1	$\overline{7}$	DATA	ODR	DATA	29 CK	SYNC	IN ACK	CLOCK	SET	CLOCK	CLR		GUARD
$\overline{29}$			EOT	EOT			$\overline{21}$	$\overline{13}$			EOT	Δ EOT			$\overline{5}$	DATA	ODR						SET	CLOCK	IN ACK		
$\overline{27}$	D_{28}	D_{24}	SHIFT	EOT	D_{20}	D_{16}	$\overline{19}$	$\overline{11}$	D_{12}	D_8	SHIFT	EOT	D_4	D_0	$\overline{3}$	SHIFT	TEST OUT ACK	Δ EOT	EOT CT	DATA GATE	CLOCK		SET	CLOCK	CLR		INTERRUPT
$\overline{25}$			SET	EOT			$\overline{17}$	$\overline{9}$			EOT	EOT			$\overline{1}$	DATA	CLR						Δ EOT	SIM D_{29}	TEST OUT ACK		
$\overline{24}$	D_{27}	D_{23}	SET	EOT	D_{19}	D_{15}	$\overline{16}$	$\overline{8}$	D_{11}	D_7	SHIFT	EOT	D_3	–	$\overline{0}$	SHIFT	PARITY	Δ EOT	EOT CT	REPEAT			ODR		CLR		INTERRUPT
D_{29}			SET	INHIBIT $\overline{29}$			$\overline{20}$	$\overline{12}$			SET				$\overline{4}$	DATA	PARITY						ODR		CLR		
																										P/L	
DI-21	SR-20	SR-20	DI-20	DC-20	SR-20	SR-20	DI-21	DI-21	SR-20	SR-20	DI-20	DC-20	SR-20	SR-20	DI-21	DI-20	DI-20	FA-20	FA-20	FA-20	DM-20	ST-30	DI-20	DI-20	DI-21	MOD	FA-20

Fig. A-8

(A-8)

C62-319

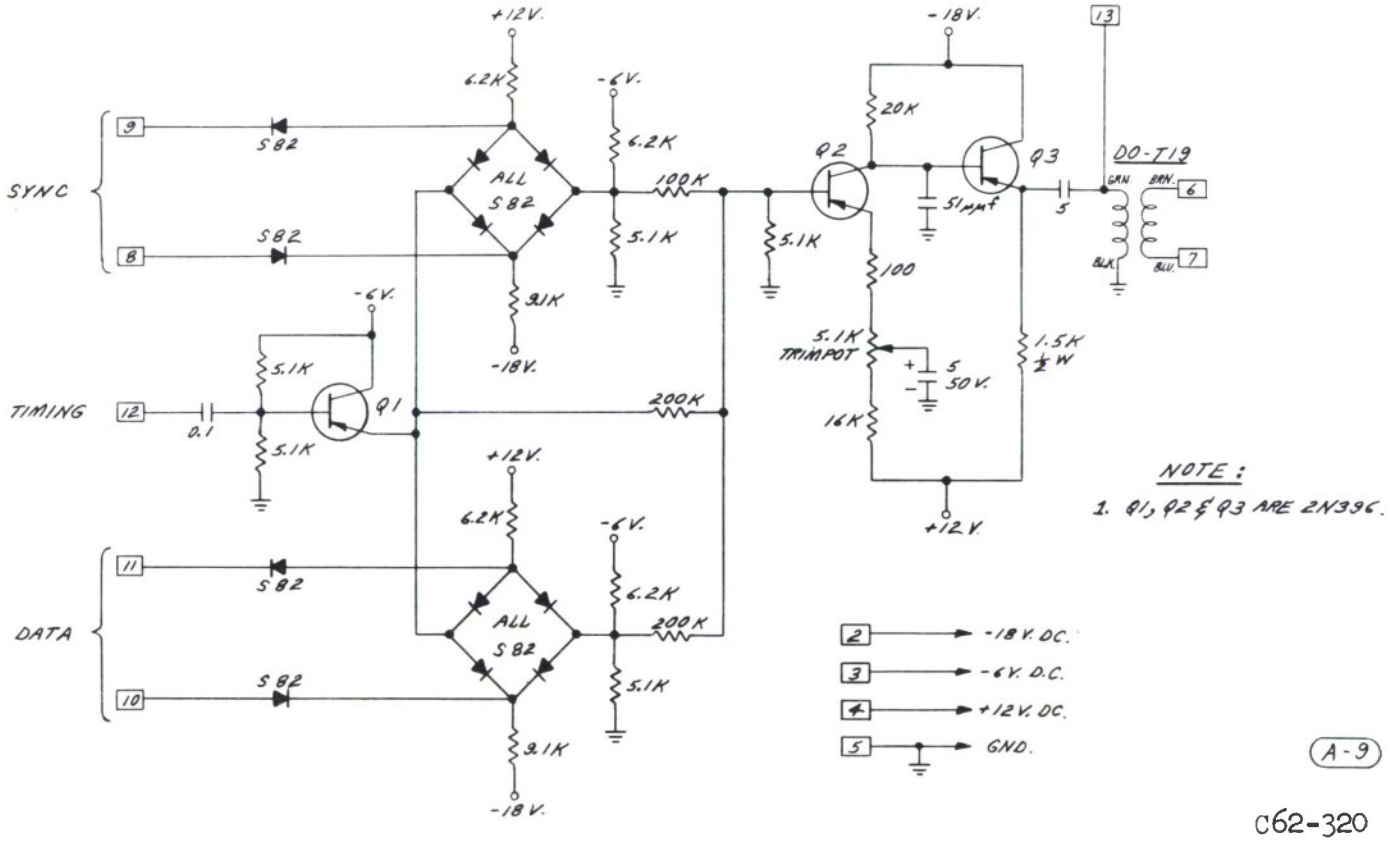

+12V.
6.2K
-6V.
SYNC
9
8
SB2
ALL SB2
100K
5.1K
9.1K
-18V.
-18V.
20K
Q2
Q3
DO-T19
GRN.
BRN.
6
7
BLK.
BLU.
13
51μμf
5
5.1K
100
5.1K TRIMPOT
5 50V.
1.5K ½W
16K
+12V.
NOTE:
1. Q1, Q2 & Q3 ARE 2N396.
-6V.
5.1K
TIMING
12
0.1
Q1
200K
5.1K
+12V.
6.2K
-6V.
DATA
11
10
SB2
ALL SB2
6.2K
200K
5.1K
9.1K
-18V.
2 → -18V. DC.
3 → -6V. D.C.
4 → +12V. DC.
5 → GND.
A-9
C62-320

Fig. A-9

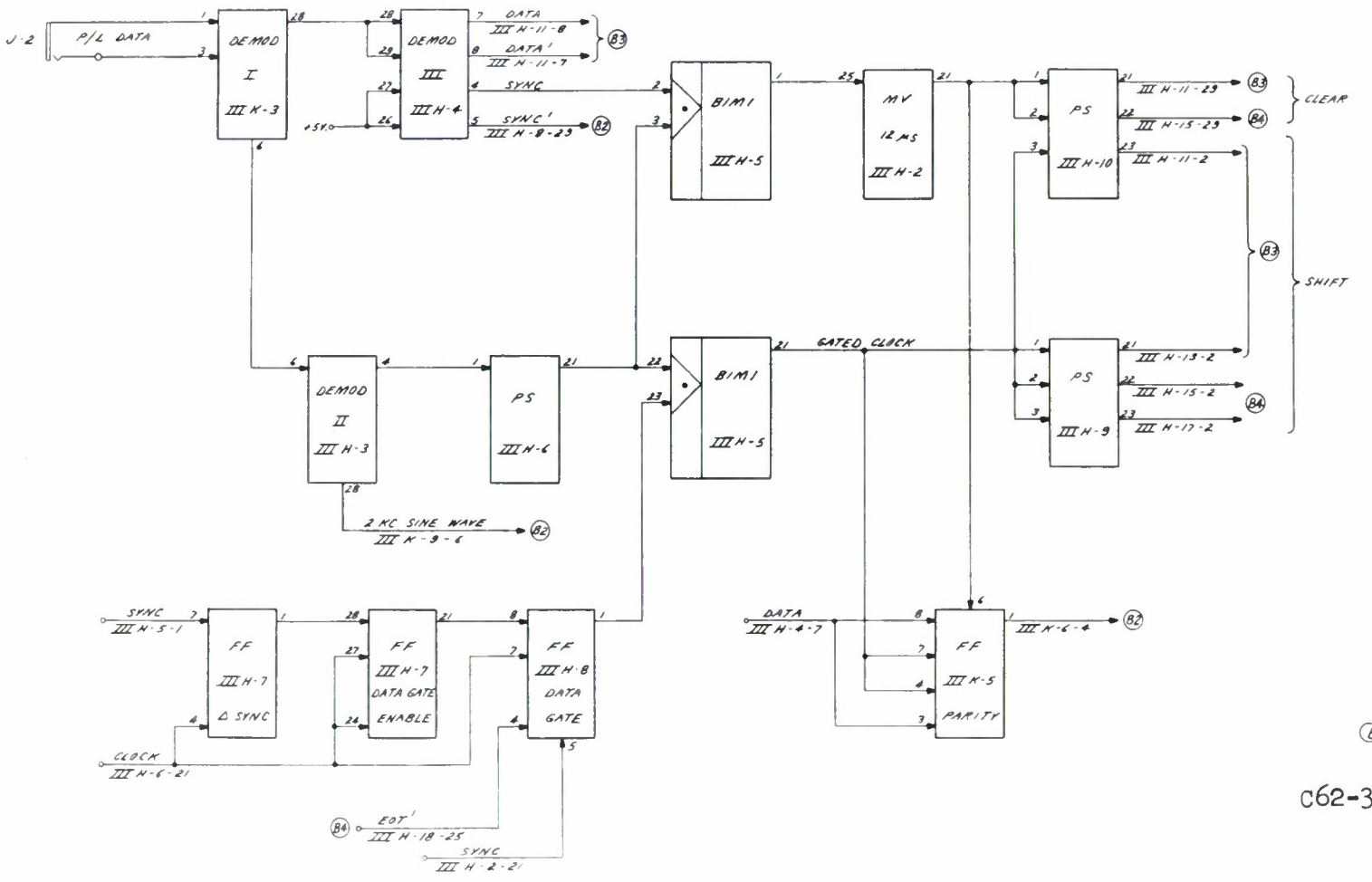

J-2
P/L DATA
DEMOD I III K-3
DEMOD III III H-4
DATA III N-11-8
DATA' III N-11-7
SYNC
SYNC' III N-8-29
+5V
BIMI III H-5
MV 12 MS III H-2
PS III H-10
III H-11-29
III H-15-29
III H-11-2
CLEAR
SHIFT
DEMOD II III H-3
PS III H-6
2 KC SINE WAVE III K-9-6
GATED CLOCK
PS III H-9
III H-13-2
III H-15-2
III H-17-2
SYNC III N-5-1
FF III H-7 Δ SYNC
FF III H-7 DATA GATE ENABLE
FF III H-8 DATA GATE
CLOCK III H-6-21
EOT' III H-18-25
SYNC III H-2-21
DATA III H-4-7
FF III K-5 PARITY
III K-6-4
B-1
C62-321

Fig. B-1

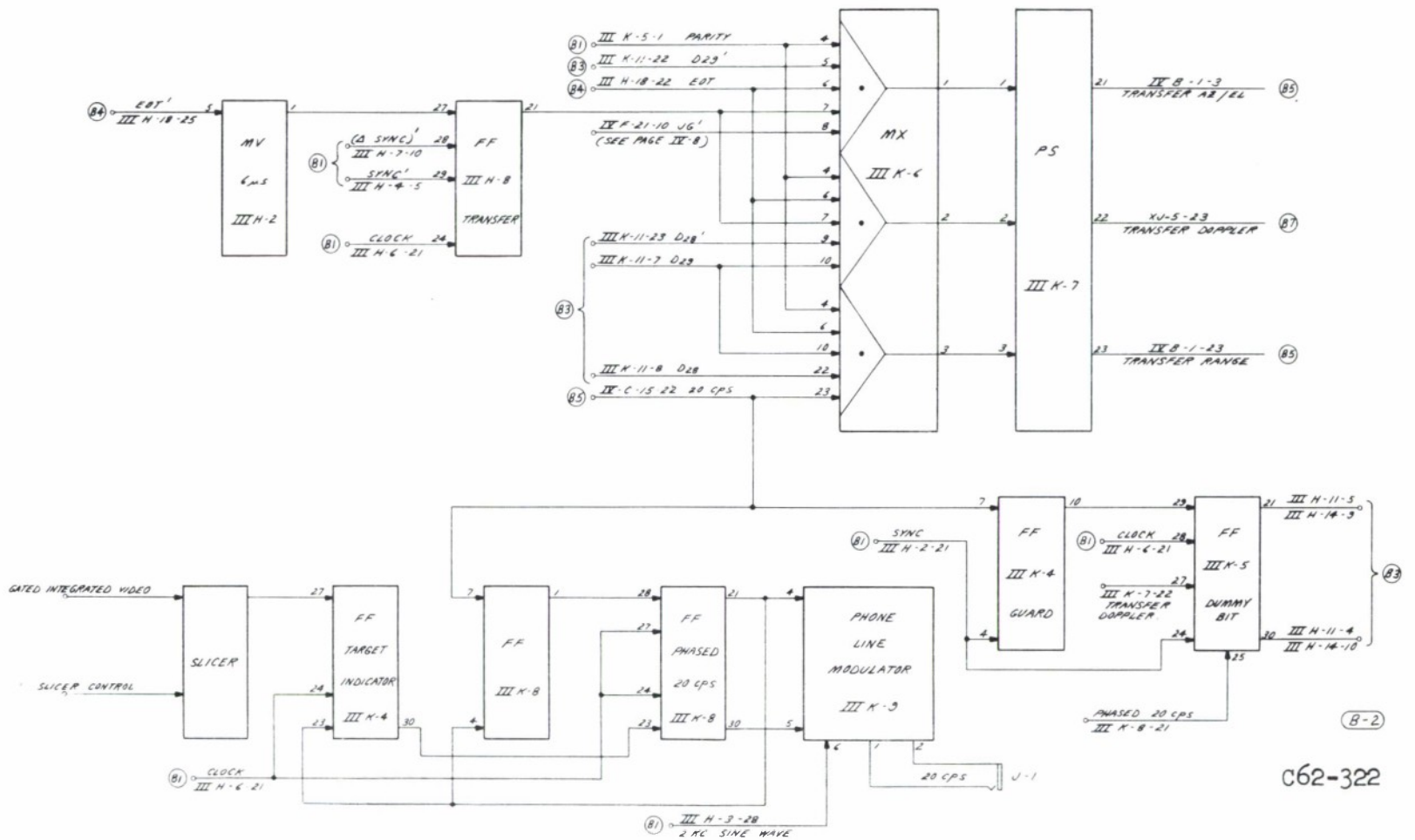

EOT'
III H-18-25
MV
6 μs
III H-2
(Δ SYNC)'
III H-7-10
SYNC'
III H-4-5
CLOCK
III H-6-21
FF
III H-8
TRANSFER
III K-5-1 PARITY
III K-11-22 D29'
III H-18-22 EOT
IX F-21-10 VG'
(SEE PAGE IX-8)
III K-11-23 D28'
III K-11-7 D29
III K-11-8 D28
IX C-15 22 20 cps
MX
III K-6
PS
III K-7
IX B-1-3
TRANSFER AZ/EL
XJ-5-23
TRANSFER DOPPLER
IX B-1-23
TRANSFER RANGE
GATED INTEGRATED VIDEO
SLICER CONTROL
SLICER
FF
TARGET
INDICATOR
III K-4
FF
III K-8
FF
PHASED
20 cps
III K-8
PHONE
LINE
MODULATOR
III K-9
20 cps
J-1
CLOCK
III H-6-21
III H-3-28
2 MC SINE WAVE
SYNC
III H-2-21
FF
III K-4
GUARD
CLOCK
III H-6-21
III K-7-22
TRANSFER
DOPPLER
FF
III K-5
DUMMY
BIT
III H-11-5
III H-14-9
III H-11-4
III H-14-10
PHASED 20 cps
III K-8-21
B-2
C62-322

Fig. B-2

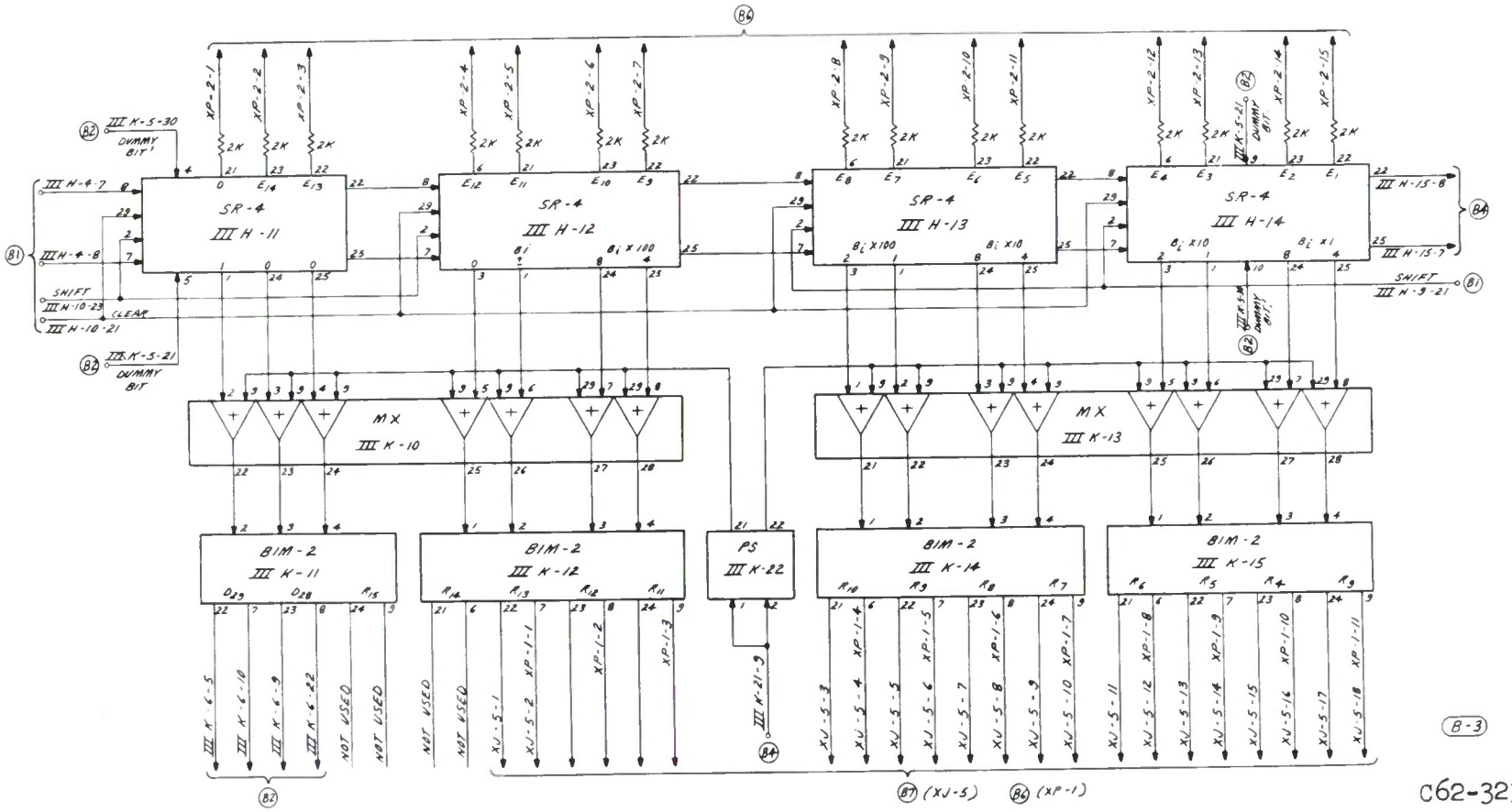

SR-4 III H-11
SR-4 III H-12
SR-4 III H-13
SR-4 III H-14
MX III K-10
MX III K-13
BIM-2 III K-11
BIM-2 III K-12
PS III K-22
BIM-2 III K-14
BIM-2 III K-15
DUMMY BIT
SHIFT III H-10-23
CLEAR III H-10-21
SHIFT III H-9-21
NOT USED
B-3
C62-323

Fig. B-3

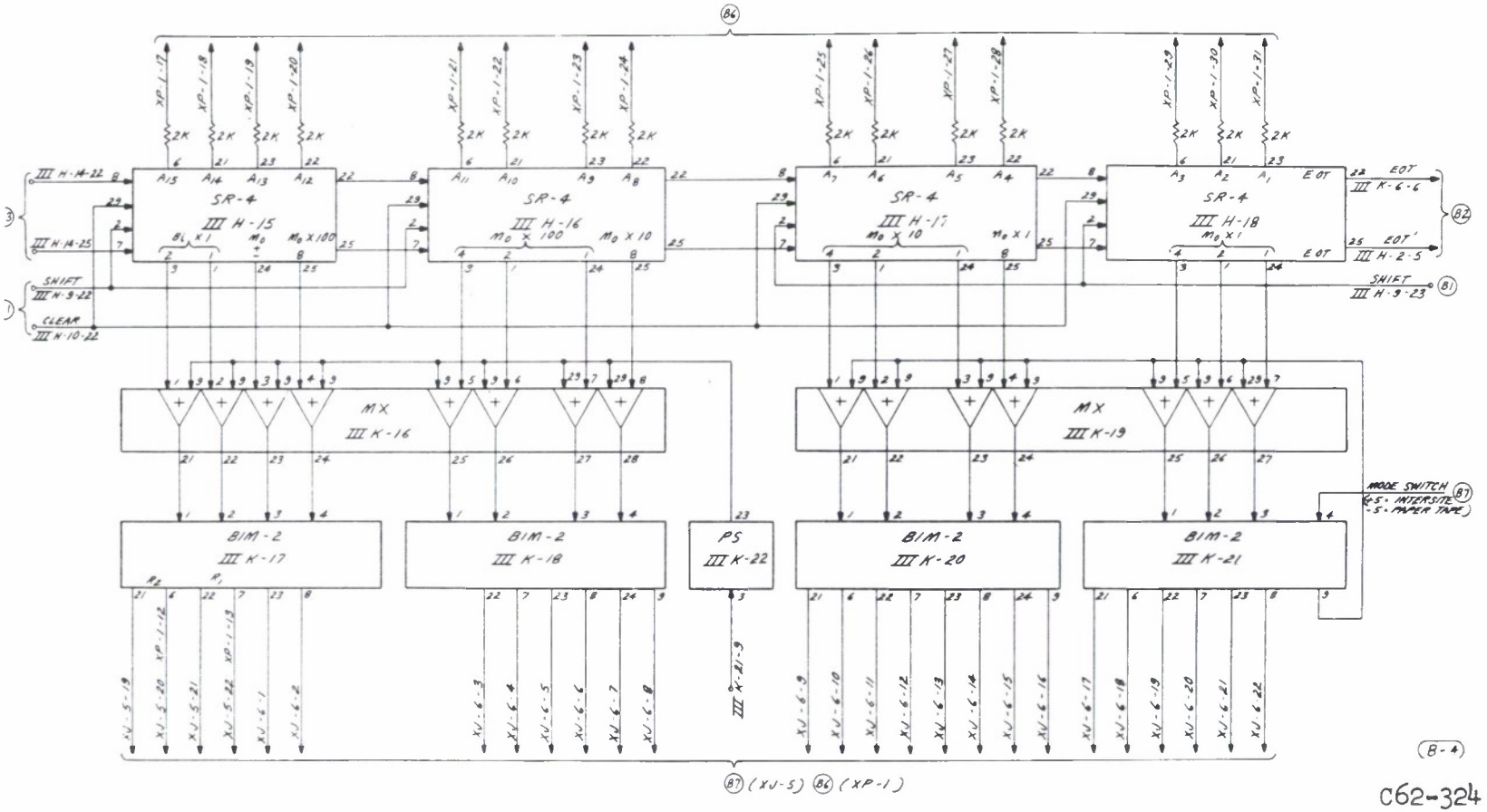
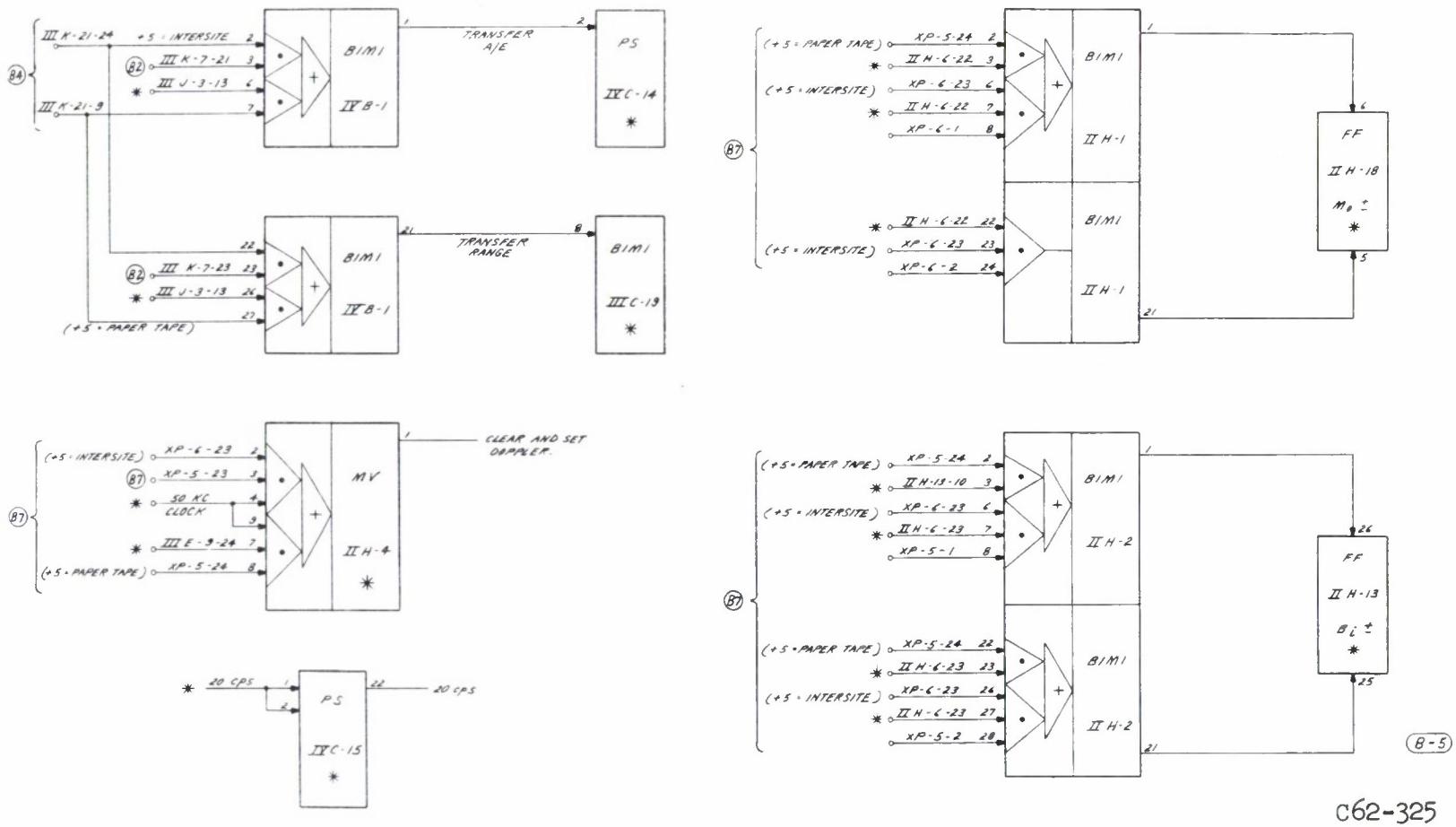

SR-4
III H-15
SR-4
III H-16
SR-4
III H-17
SR-4
III H-18
MX
III K-16
MX
III K-19
BIM-2
III K-17
BIM-2
III K-18
PS
III K-22
BIM-2
III K-20
BIM-2
III K-21
SHIFT
CLEAR
EOT
MODE SWITCH
(87) (XJ-5) (86) (XP-1)
C62-324

Fig. B-4



C62-325

Fig. B-5

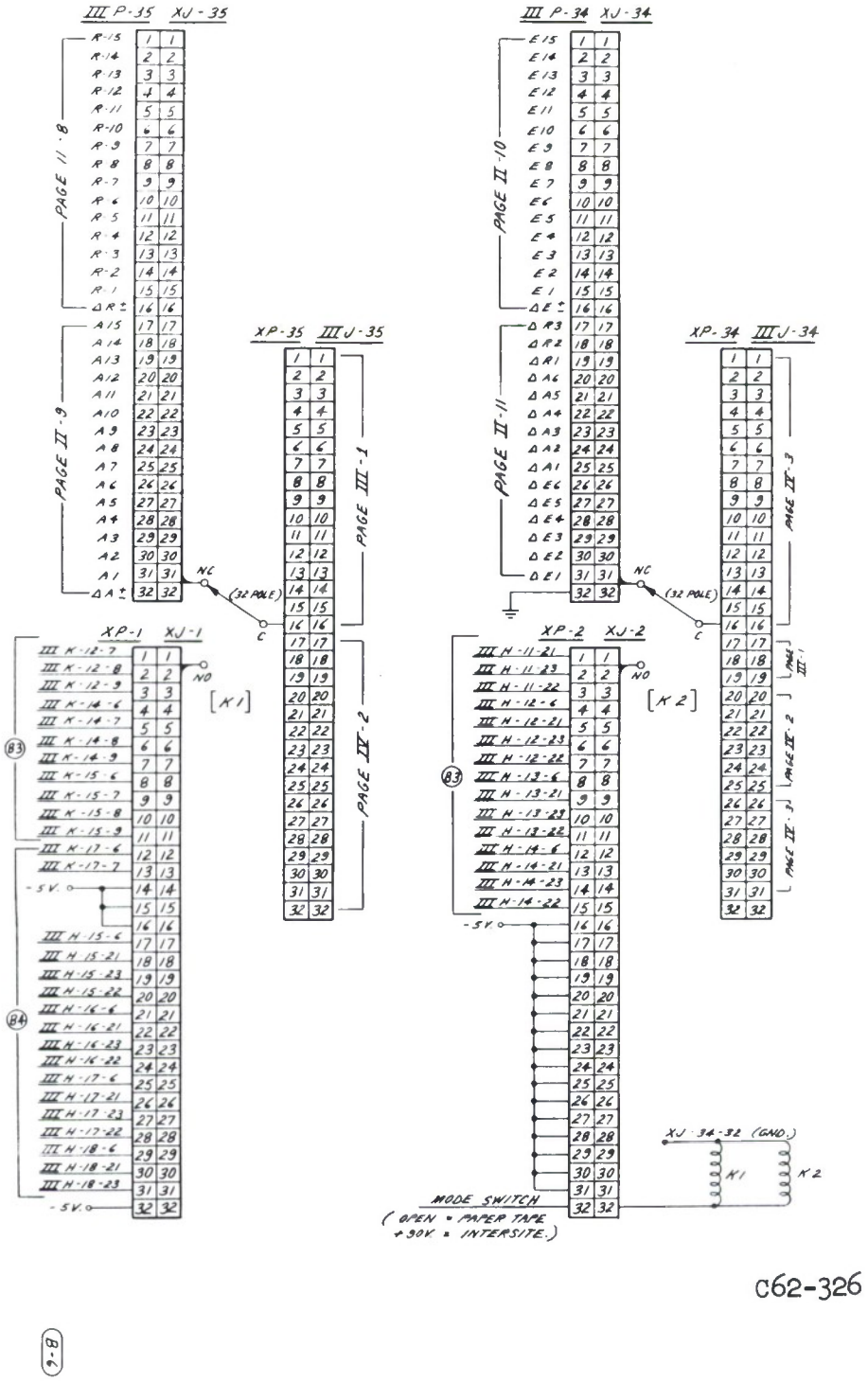

III P-35 XJ-35
PAGE II-8
PAGE II-9
XP-35 IIIJ-35
PAGE III-1
PAGE III-2
NC
NO
C
(32 POLE)
XP-1 XJ-1
[K1]
-5V.
B3
B4
III P-34 XJ-34
PAGE II-10
PAGE II-11
XP-34 IIIJ-34
PAGE III-3
XP-2 XJ-2
[K2]
MODE SWITCH
(OPEN = PAPER TAPE
+90V = INTERSITE.)
XJ-34-32 (GND.)
K1
K2
C62-326
9-8

Fig. B-6

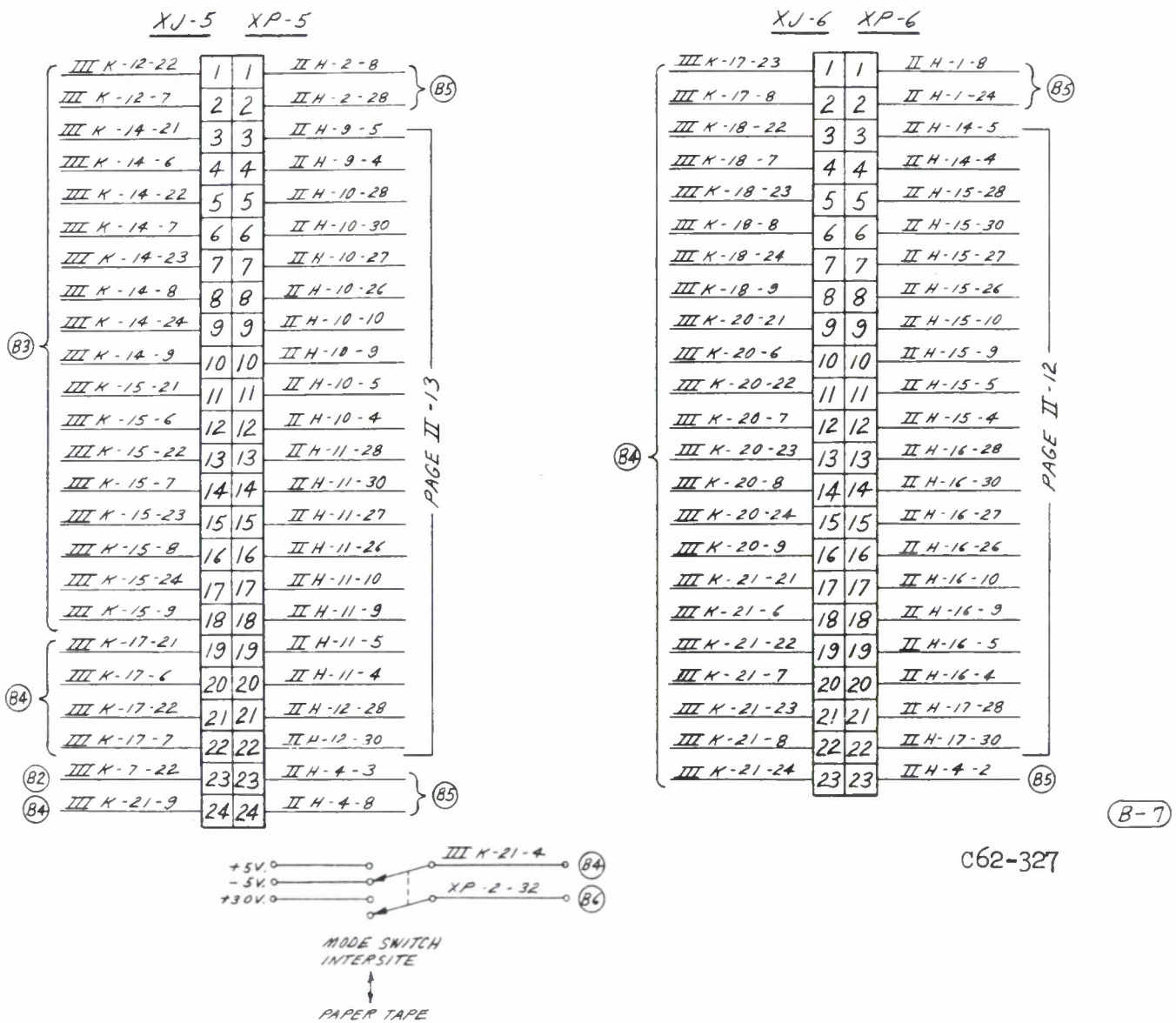
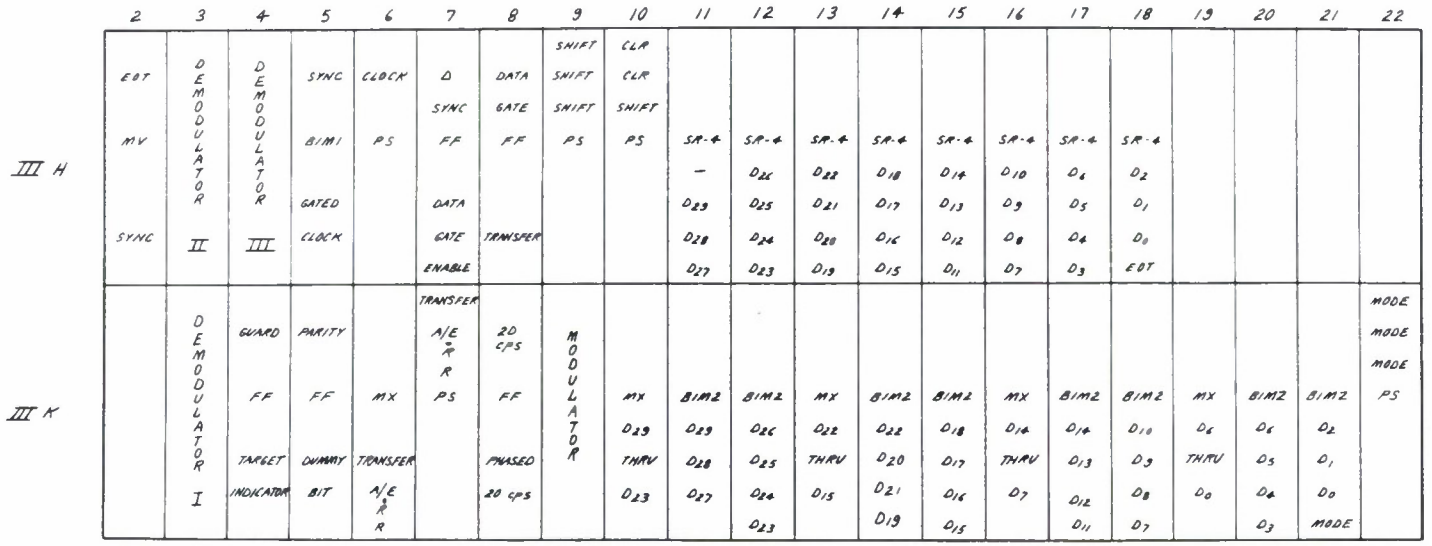

XJ-5
XP-5
III K-12-22
III K-12-7
III K-14-21
III K-14-6
III K-14-22
III K-14-7
III K-14-23
III K-14-8
III K-14-24
III K-14-9
III K-15-21
III K-15-6
III K-15-22
III K-15-7
III K-15-23
III K-15-8
III K-15-24
III K-15-9
III K-17-21
III K-17-6
III K-17-22
III K-17-7
III K-7-22
III K-21-9
II H-2-8
II H-2-28
II H-9-5
II H-9-4
II H-10-28
II H-10-30
II H-10-27
II H-10-26
II H-10-10
II H-10-9
II H-10-5
II H-10-4
II H-11-28
II H-11-30
II H-11-27
II H-11-26
II H-11-10
II H-11-9
II H-11-5
II H-11-4
II H-12-28
II H-12-30
II H-4-3
II H-4-8
B3
B4
B2
B4
B5
B5
PAGE II-13
XJ-6
XP-6
III K-17-23
III K-17-8
III K-18-22
III K-18-7
III K-18-23
III K-18-8
III K-18-24
III K-18-9
III K-20-21
III K-20-6
III K-20-22
III K-20-7
III K-20-23
III K-20-8
III K-20-24
III K-20-9
III K-21-21
III K-21-6
III K-21-22
III K-21-7
III K-21-23
III K-21-8
III K-21-24
II H-1-8
II H-1-24
II H-14-5
II H-14-4
II H-15-28
II H-15-30
II H-15-27
II H-15-26
II H-15-10
II H-15-9
II H-15-5
II H-15-4
II H-16-28
II H-16-30
II H-16-27
II H-16-26
II H-16-10
II H-16-9
II H-16-5
II H-16-4
II H-17-28
II H-17-30
II H-4-2
B4
B5
B5
PAGE II-12
B-7
+5V.
-5V.
+30V.
III K-21-4
XP-2-32
B4
B6
MODE SWITCH
INTERSITE
PAPER TAPE
C62-327

Fig. B-7



C62-328

B-8

Fig. B-8

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